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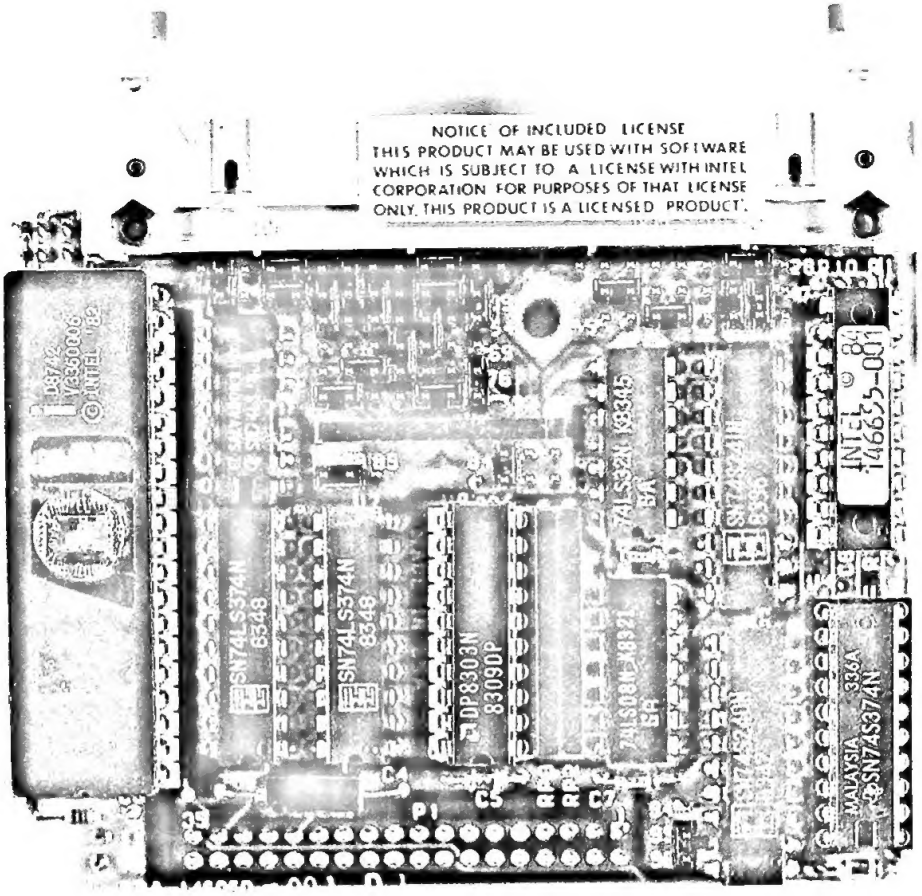
iSBX™ 217C MAGNETIC CARTRIDGE TAPE INTERFACE MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL



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Order Number: 146704-001

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PREFACE

This manual describes the iSBX 217C Magnetic Cartridge Tape Interface MULTIMODULE board. The manual explains how to use the features associated with a typical tape drive installation using either the QIC-Ø2 (Quarter Inch Cartridge-Ø2) or 3M HCD-75 interface. For additional information, the following publications are available from the Intel Literature Department:

- Intel MULTIBUS® Specification, Order Number: 98ØØ683
- Intel iSBX™ Bus Specification, Order Number: 145695

To obtain the latest copy of the QIC-Ø2 Intelligent Interface Standard for 1/4 inch Cartridge Tape Drives, contact either the manufacturer of the tape drive or the:

Archive Corporation
354Ø Cadillac Avenue
Costa Mesa, CA. 92626
(714) 641-Ø279

To obtain the latest copy of the 3M HCD-75 Interface Standard for High Capacity Data Cartridge Drive Systems, contact:

Data Products/3M
223-5E 3M Center
St. Paul, MN 55144
(612) 733-8892

NOTE

Throughout this manual, an asterisk (*) following a signal name means that the signal is active-low. Former Intel manuals and schematic diagrams use a slash (/) to denote active-low signals.

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The iSBX 217C Magnetic Cartridge Tape Interface Board is an 8-bit, single-wide, iSBX MULTIMODULE I/O expansion board for installation on any 8-bit or 16-bit iSBC host board which has an iSBX connector. Its function is to interface industry-standard 1/4 inch magnetic cartridge tape drives to a host MULTIBUS processor board. The iSBX 217C board supports the QIC-Ø2 (Quarter Inch Cartridge-Ø2) streaming tape drive interface, and the 3M Company HCD-75 interface. Each iSBX 217C board can support up to four tape drives (of the same manufacturer).

This manual provides the installation and setup information you need to interface the iSBX 217C board with a host iSBC board and a magnetic cartridge tape drive. Required interfacing information is provided in Chapter 3, and service information is covered in Chapter 4.

1.2 DESCRIPTION

The iSBX 217C board is designed to handle the interface and transfer of data from an iSBC host board such as the iSBC 215G Winchester Disk Controller board, to a 1/4 inch magnetic tape cartridge device. The transfer may occur in one of two modes: direct memory access (DMA) mode or a high-speed programmed I/O mode.

Three types of drives can be used with the iSBX 217C board: the high-speed, 9Ø inch-per-second (ips) QIC-Ø2 drive; the 3Ø ips QIC-Ø2 drive; and the 3M Company's HCD-75 drive. To use the 9Ø ips QIC-Ø2 drive, the host board must be capable of transferring data at 1ØØK bytes/second or faster, or have DMA capability. Using the slower, 3Ø ips QIC-Ø2 drive, or the 3M drive is possible with any Intel host board, using either DMA or programmed I/O.

As with all other iSBX MULTIMODULE boards, the iSBX 217C board plugs directly onto the host iSBC board via the iSBX bus connector. This enables the iSBX board to communicate directly with the host board via the internal iSBX bus. All Intel iSBC boards with an iSBX connector support the required command and status signals for proper iSBX 217C board operation. Board power (+5VDC @ 1.5Ø amps) is provided by the host iSBC board, via the iSBX connector.

The tape drive interfaces to the iSBX 217C board through a single 5Ø-pin connector (J1). The board is factory-configured for the QIC-Ø2 tape drive interface; you can reconfigure the board for the 3M Company drive by changing the jumper matrix configuration and installing several wires.

1.3 EQUIPMENT SUPPLIED

The iSBX 217C board is shipped from the factory with several pieces of plastic mounting hardware and a schematic diagram. The mounting hardware is used to secure the iSBX board to the iSBC host board. Installation instructions are provided in Chapter 2. The schematic diagram should be saved for future reference since it may be more current than the diagram in Chapter 4. Connectors and cable pieces are not supplied with the board. Connector information is provided in Chapter 2.

1.4 SPECIFICATIONS

Board specifications are listed in Table 1-1.

Table 1-1. Board Specifications

Physical Dimensions	
Width:	3.7Ø inches (9.4 cm)
Length:	3.Ø7 inches (7.8 cm)
Height:	Ø.8Ø inch (2.Ø cm); see Figure 2-2
Weight:	3.5 ounces (98.Ø gm)
Current Requirements	+5V @ 1.5 A Maximum
Environmental Characteristics	
Operating Temperature:	Ø°C to 55°C
Storage Temperature:	-4Ø°C to 85°C
Humidity:	5Ø% to 95% non-condensing @ 25°C to 4Ø°C
Vibration & Shock:	2G maximum through 5ØHz
Minimum Airflow:	2ØØ linear ft./min. per board position at inlet temperature of less than 55°C

***

CHAPTER 2
PREPARATON FOR USE

2.1 INTRODUCTION

This chapter provides installation instructions and configuration information for the iSBX 217C board. The information presented in this chapter includes unpacking and inspection instructions; installation considerations such as physical dimensions, cooling requirements, and mounting instructions; connector pin assignments; and jumper configurations.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service HOTLINE to obtain a return authorization number and further instructions (see section 4.2). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2.3 INSTALLATION CONSIDERATIONS

The following sections provide installation information for the iSBX 217C board.

2.3.1 PHYSICAL DIMENSIONS

Physical dimensions of the iSBX 217C board are provided in Figure 2-1. Mounting clearance detail is shown in Figure 2-2.

NOTE

In some cardcage models, the host iSBC and iSBX board combination uses two slots.

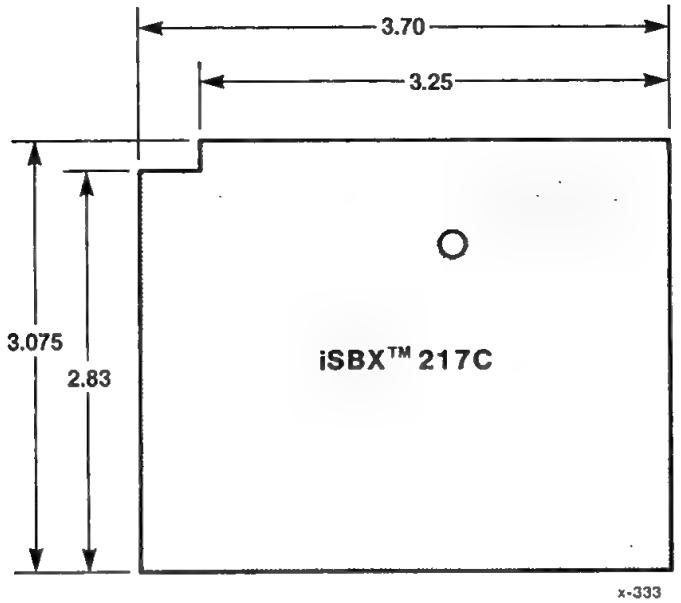

Figure 2-1. Physical Dimensions (Inches)

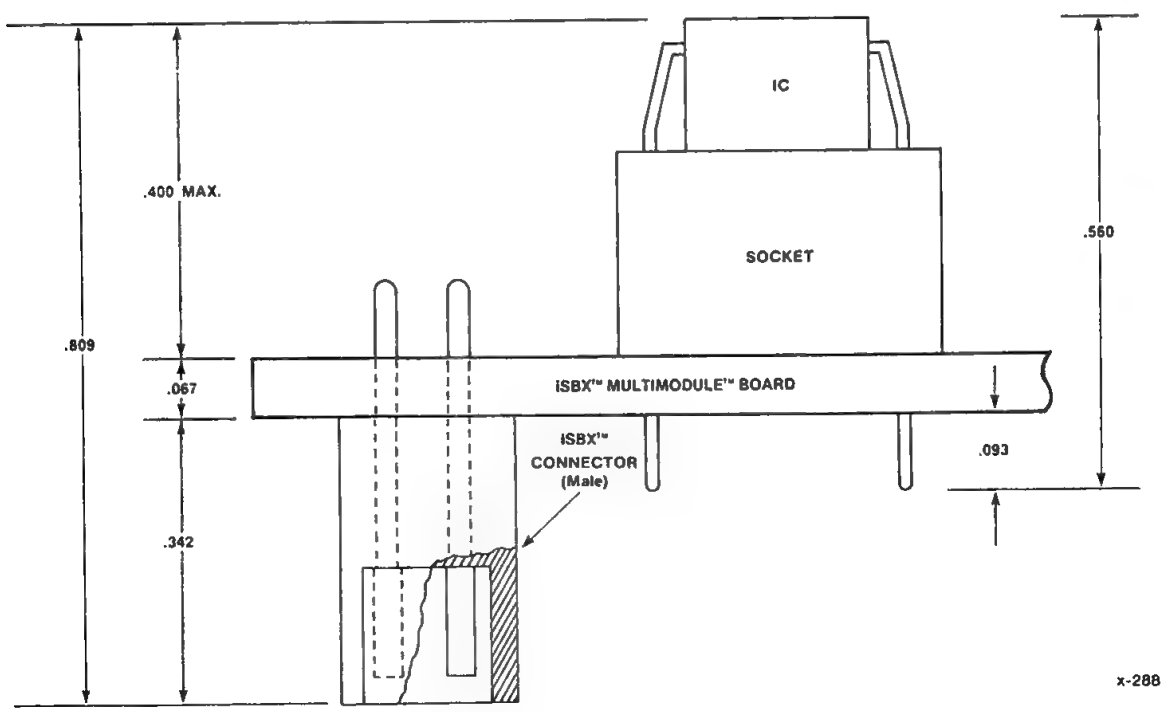

Figure 2-2. Mounting Clearances (Inches)

2.3.2 POWER REQUIREMENTS

The iSBX 217C board requires +5VDC @ 1.5A. The host iSBC board supplies power through the iSBX connector.

2.3.3 COOLING REQUIREMENTS

A minimum airflow of 2ØØ linear feet/minute per board position, at an inlet temperature of less than 55°C, is required for sufficient cooling.

2.3.4 GENERAL SYSTEM REQUIREMENTS

A user-provided program, running on the host board, must be used to handle the command, status, and data exchange between the iSBX 217C board and the host board. Host boards without DMA capability must use a programmed I/O routine to read/write commands and data to/from the iSBX 217C board. A host board that supports direct memory access (DMA) operations can use either the DMA mode or the programmed I/O mode. Refer to Chapter 3 for specific programming and interfacing information.

The iSBX 217C board can be used on any host iSBC board with an iSBX MULTIMODULE connector. However, in order to use the high-speed, 9Ø-inch per second QIC-Ø2 drive, the host board must have either DMA capability, or be capable of transferring data at 1ØØK bytes/second or faster. If you are using the cartridge tape drive for hard disk backup or program loading onto a hard disk, then the iSBX 217C board is ideally suited for use on the iSBC 215G Winchester Disk Controller Board.

2.4 JUMPER CONFIGURATIONS

Jumpers are used to define the type of tape drive in use. Table 2-1 and Figure 2-3 summarize the jumper configuration for the QIC-Ø2 interface drive (factory default configuration). Table 2-2 and Figure 2-4 give the jumper configuration for the 3M drive interface.

NOTE

If the QIC-Ø2 drive being used with the iSBX 217C board does not support the optional QIC-Ø2 parity signal (HBP*), the iSBX 217C board must be reconfigured to disable the parity checking circuitry.

1. Remove jumper 87-88 (LPAR).
2. Remove jumper 37-38 (HBP*).
3. Remove jumper 95-96 (OE*).
4. Add wire wrap jumper from 88 to 96.
5. Add wire wrap jumper from 95 to 96.

Table 2-1. QIC-Ø2 Interface Factory Default Jumper Configurations

Name	From	To	Comments
RP2-4	E84	E91	Connect RP2-4
OE*	E95	E96	Ground OE*
D7	E1Ø	E11	Data bit 7
D6	E13	E34	Data bit 6
D5	E31	E32	Data bit 5
D4	E16	E17	Data bit 4
D3	E52	E67	Data bit 3
D2	E35	E5Ø	Data bit 2
D1	E33	E48	Data bit 1
DØ	E71	E72	Data bit Ø
OUTØ*	E39	E54	Connect OUTØ* to ONLINE*
OUT1*	E66	E73	Connect OUT1* to REQ*
RESET*	E46	E61	Connect RESET*
XFER*	E57	E58	Connect XFER*
ACKØ*	E45	E6Ø	Connect ACKØ* to ACK*
INØ*	E4Ø	E41	Connect INØ* to RDY*
IN1*	E26	E27	Connect IN1* to EXCEPTION*
HBP*	E37	E38	Connect Parity Line
BPL*	E81	E82	Connect BPL to IN3
PAL13*	E77	E78	Connect PAL12 to PAL13
LPAR	E87	E88	Connect LPAR to ACK1* (ODD)
Chassis GND	E8	E29	Connect Signal GND to Chassis GND

Note: Jumper connections are made with push-on headers.

If the QIC-Ø2 interface drive being used with the iSBX 217C board does not support the optional QIC-Ø2 parity signal (HBP*), the iSBX 217C board must be reconfigured to disable the parity checking circuitry (see Section 2.4).

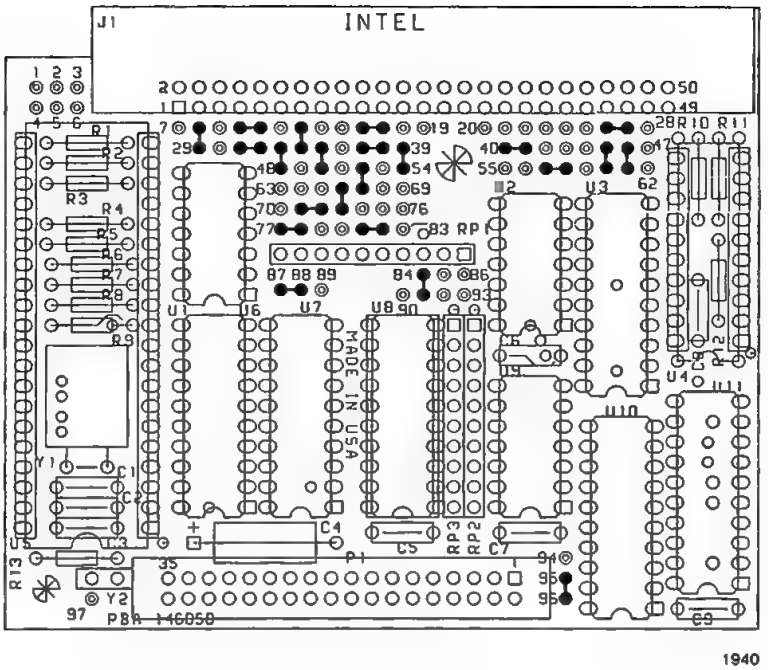

Figure 2-3. QIC-Ø2 Jumper Configuration

2.4.1 CONVERSION TO 3M DRIVE INTERFACE

To convert the iSBX 217C board from the default QIC-Ø2 interface, to the 3M interface, follow these steps:

1. Remove all push-on jumper connectors from the board.

2. Install the wire-wrap jumpers as shown in Table 2-2 and Figure 2-4.

3. Insert the push-on jumpers as shown in Table 2-2 and Figure 2-4.

4. Remove resistor pack RN3 on the 3M drive to prevent overloading the iSBX 217C data bus lines. Refer to the 3M drive manual for exact location of component.

5. Remove the socketed device at location U4 (see Figure 2-4). Program a blank PAL16R6 device with the PALASM† source code contained in Appendix B. Install the PAL16R6 device in location U4. Ensure that pin 1 of the device is oriented with pin 1 of the socket. The PALASM assembler and blank PAL16R6 devices can be obtained from Monolithic Memories, Inc.

† = PALASM is a registered trademark of Monolithic Memories, Inc.

Table 2-2. 3M Interface Jumper Configurations

Name	From	To	Comments
D7	E11	E12	Connect D7 to low byte;
	E5Ø	E65	high byte
D6	E13	E14	Connect D6 to low byte;
	E48	E63	high byte
D5	E3Ø	E31	Connect D5 to low byte;
	E64	E71	high byte
D4	E17	E38	Connect D4 to low byte;
	E53	E54	high byte
D3	E9	E1Ø	Connect D3 to low byte;
	E66	E67	high byte
D2	E34	E35	Connect D2 to low byte;
	E18	E19	high byte
D1	E32	E33	Connect D1 to low byte;
	E79	E8Ø	high byte
DØ	E15	E16	Connect DØ to low byte;
	E72 #	E74	high byte
RESET	E7	E8	Connect RESET* to INIT*
PAL12*	E2 #	E52	Connect U1Ø-7 to Byte 2
	E24	E37 #	Connect U1Ø-13 to PAL12*
PAL19*	E28	E56 #	Connect PAL 19* to U1Ø-11
	E1	E41 #	Connect U1Ø-9 to Byte 1
XFER*-P2	E3	E6	Connect XFER* to P2
OUTØ*	E21	E39 #	Connect OUTØ* to RDY
OUT1*	E25	E44	Connect OUT1* to C/D
W/R	E47	E62	Connect W/R to I/O
XFER*	E23	E22	Connect XFER* to ACK
ACKØ*	E43 #	E6Ø	Connect ACKØ* to REQ
ACK1*	E76	E83	Connect ACK1* to OUT3*
IN1*	E26	E43 #	Connect IN1* to REQ
INØ*	E36	E49 #	Connect INØ* to ATN
OE*	E94	E95	Connect OE* to GND

Notes: Jumper connections are made with push-on headers, except as noted.

= Wire wrap jumpers.

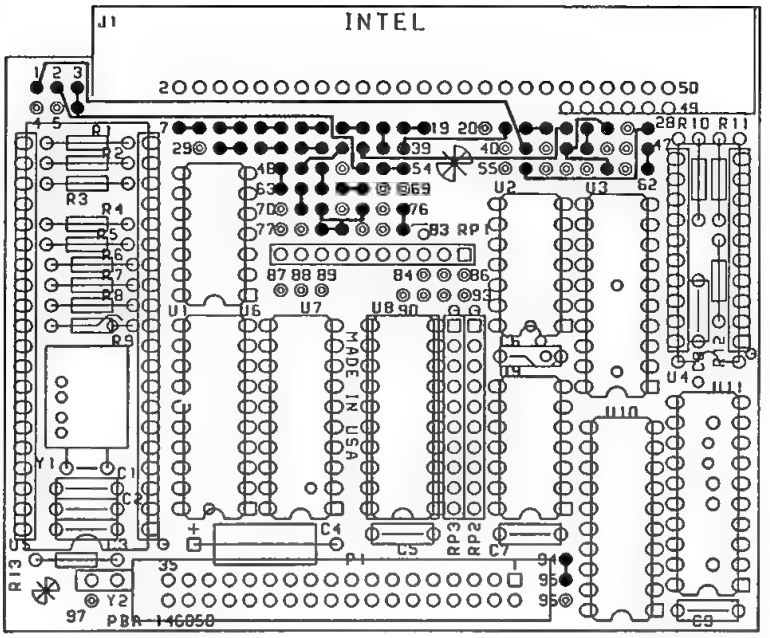

Figure 2-4. 3M Jumper Configuration

2.5 CABLE AND CONNECTOR INFORMATION

Edge connector J1 is used to connect the tape drive to the iSBX 217C board. This connector is a 3M Company 5Ø-pin, right angle header, part number 3433. It mates to the 3M Company connector, part number 3425. Equivalent mating connectors from other vendors are available. Maximum cable length from the board to the drive is 3 meters (1Ø feet). A daisy chain cable must be used for multiple drives (up to four drives).

2.6 CONNECTOR J1 PIN IDENTIFICATION

This section provides a pin-out diagram and gives signal definitions for connector J1. The signals present on the J1 pins depend on the jumper configuration of the iSBX 217C board. Table 2-3 provides pin/signal names; Table 2-4 provides signal definitions, when the board is configured for the QIC-Ø2 interface; Table 2-5 provides signal definitions for the 3M interface.

NOTE

In the 3M configuration, ensure that pin 1 of board connector is connected to pin 5Ø of the drive cable. See Table 2-3.

CAUTION

Remove resistor pack RN3 on the 3M drive to prevent overloading the iSBX 217C board data bus lines. Refer to the 3M drive manual for exact location of component.

Table 2-3. Connector J1 Pin Assignments

217C Pin	QIC-Ø2 Interface		3M Interface		217C Pin	QIC-Ø2 Interface		3M Interface	
	Pin	Function	Pin	Function		Pin	Function	Pin	Function
1	1	GND	5Ø	RESET	2	2	NC	49	INØ*
3	3	OPEN	48	OPEN	4	4	NC	47	D7 LOW
5	5	OPEN	46	OPEN	6	6	NC	45	D6 LOW
7	7	OPEN	44	OPEN	8	8	NC	43	D5 LOW
9	9	GND	42	GND	1Ø	1Ø	HBP	41	D4 LOW
11	11	GND	4Ø	GND	12	12	D7	39	D3 LOW
13	13	GND	38	GND	14	14	D6	37	D2 LOW
15	15	GND	36	GND	16	16	D5	35	D1 LOW
17	17	GND	34	GND	18	18	D4	33	DØ LOW
19	19	GND	32	GND	2Ø	2Ø	D3	31	PAL12
21	21	GND	3Ø	GND	22	22	D2	29	D7 HIGH
23	23	GND	28	GND	24	24	D1	27	D6 HIGH
25	25	GND	26	GND	26	26	DØ	25	D5 HIGH
27	27	GND	24	GND	28	28	OUTØ*	23	D4 HIGH
29	29	GND	22	GND	3Ø	3Ø	OUT1*	21	D3 HIGH
31	31	GND	2Ø	GND	32	32	RESET*	19	D2 HIGH
33	33	GND	18	GND	34	34	XFER*	17	D1 HIGH
35	35	GND	16	GND	36	36	ACKØ*	15	DØ HIGH
37	37	GND	14	GND	38	38	INØ*	13	PAL19
39	39	GND	12	GND	4Ø	4Ø	IN1*	11	NC
41	41	GND	1Ø	GND	42	42	NC	9	OUTØ*
43	43	GND	8	GND	44	44	NC	7	OUT1*
45	45	GND	6	GND	46	46	NC	5	W/R
47	47	GND	4	GND	48	48	NC	3	XFER*
49	49	GND	2	GND	5Ø	5Ø	NC	1	ACKØ* and IN1*

Notes: QIC-Ø2 = Shipped default configuration;

NC = no connection;

* = active low.

Table 2-4. Connector J1 Signal Definitions - QIC-Ø2 Configuration

HBØ-HB7:	Bi-directional data bus. (DØ-D7) HBØ is the least significant bit.
HBP:	Bi-directional parity line (odd).
ONL:	Online (OUTØ*) - iSBX 217C board generated control signal which is activated prior to transferring a Read and Write command.
REQ:	Request (OUT1*) - iSBX 217C board generated control signal which indicates that command data has been placed on the data bus in command mode or that status has been taken from the data bus in status mode.
XFER:	Transfer (XFER*) - iSBX 217C board generated control signal which indicates that data has been placed on the data bus in write mode or that data has been taken from the data bus in read mode.
ACK:	Acknowledge (ACKØ*) - drive generated signal which indicates that data has been taken from the data bus in Write Mode or that data has been placed on the data bus in Read Mode.
RDY:	Ready (INØ*) - drive generated signal which indicates the following: 1) If no operation is in progress, RDY means ready to accept a command. 2) Data has been taken from the data bus in command mode. 3) Data has been placed on the data bus in status mode. 4) A buffer is ready to be filled by the host in write mode. 5) A buffer is ready to be emptied by the host in read mode. 6) A position command has been completed in position mode. 7) At the conclusion of a write file mark.
EXC:	Exception (IN1*) - drive generated signal which indicates that an error condition occurred during a file mark cycle or on reset.
RES:	Reset (RESET*) - iSBX 217C board generated signal that causes the drive to perform a power-on sequence

Note: QIC-Ø2 signal names shown in leftmost column; iSBX 217C signal names are shown in parenthesis.

Table 2-5. Connector J1 Signal Definitions - 3M Configuration

DØ - D7:	Data Input Bus/Data Output Bus: 16 lines for the bi-directional 3M bus. The two buses are tied together and, along with the byte 1 and byte 2 control signals, allow the 8-bit directional iSBX 217C board to control the HCD-75 tape drive.
C/D:	Command/Data (OUT1*) - a iSBX 217C board generated signal that is used to indicate (to the drive) whether information on the bus is a command to be executed or data to be written. Set high to indicate a command and low for a data transfer.
I/O:	Input/Output ($W/\overline{R}$) - a iSBX 217C board generated signal that is used to control the direction of transfers between the iSBX 217C board and the drive. Set high for direction flow to the drive and low for direction flow to the iSBX 217C board.
RDY:	Ready (OUTØ*) - a iSBX 217C board generated signal that is set low when the iSBX 217C board is initiating a command, data, or status transfer.
INIT:	Initialize (RESET*) - a iSBX 217C board generated signal that, when pulsed high, resets the drive and puts the drive in a ready state.
ATN:	Attention (INØ*) - a drive generated signal which is set high to indicate an attention condition to read the drive status.
REQ:	Transfer Request (ACKØ* and IN1*) - an input to the iSBX 217C board that is set low (by the drive) when the drive is ready to accept data during write operations or when data becomes valid during read operations.
ACK:	Transfer Acknowledge (XFER*) - an output from the iSBX 217C board that strobes high when valid data is on the bus during a write operation or when the host has read a byte of data during a read operation.
BYTE1:	Byte 1 Control (PAL19*) - an output from the iSBX 217C board that strobes the low byte of the drive 16-bit bus.
BYTE2:	Byte 2 Control (PAL12*) - an output from the iSBX 217C board that strobes the high byte of the drive 16-bit bus.

Note: 3M drive signals are shown in leftmost column; iSBX 217C signal names are shown in parenthesis.

2.7 iSBX™ MULTIMODULE™ CONNECTOR

Pin assignments for connector P1 (iSBX MULTIMODULE) are listed in Table 2-6. Signals which end with a slash (/) or asterisk (*) are active-low TTL signals; signals without a slash or asterisk are active-high.

NOTE

Ensure that the host board is not driving MINTR1 (pin 12). The iSBX 217C board drives MINTR1, but the host board should not interpret this as an interrupt.

Table 2-6. iSBX™ Bus Connector Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+12V #	+12 Volts	2	-12V #	-12 Volts
3	GND	Signal Ground	4	+5V	+5 Volts
5	RESET	Reset	6	MCLK	M Clock
7	MA2 #	M Address 2	8	MPST*	iSBX Bd Present
9	MA1 #	M Address 1	1Ø	--	Reserved
11	MAØ	M Address Ø	12	MINTR1 #	M Interrupt 1
13	IOWRT*	IO Write Cmd	14	MINTRØ	M Interrupt Ø
15	IORD*	IO Read Cmd	16	MWAIT*	M Wait
17	GND	Signal Ground	18	+5V	+5 Volts
19	MD7	M Data Bit 7	2Ø	MCS1*	M Chip Select 1
21	MD6	M Data Bit 6	22	MCSØ*	M Chip Select Ø
23	MD5	M Data Bit 5	24	--	Reserved
25	MD4	M Data Bit 4	26	--	Reserved
27	MD3	M Data Bit 3	28	OPTØ	Option Ø
29	MD2	M Data Bit 2	3Ø	OPT1	Option 1
31	MD1	M Data Bit 1	32	--	Reserved
33	MDØ	M Data Bit Ø	34	--	Reserved
35	GND	Signal Ground	36	+5V	+5 Volts

Note: # = not used by iSBX 217C board.

2.8 INSTALLATION PROCEDURE

The iSBX 217C board can be easily installed without special equipment or tools. The following procedure outlines iSBX 217C board installation:

CAUTION

The host iSBC board must be removed from chassis or cardcage for proper installation of the iSBX 217C board. Turn off power before removal.

a. Some iSBC Single Board Computers have up to three iSBX MULTIMODULE connectors. Choose the connector location which corresponds to the host I/O addressing you select. Avoid using the rightmost iSBX connector if possible; the iSBX 217C board J1 connector latch may not open correctly with some cardcage models.

   Refer to Table 3-4 or to the host board hardware reference manual for the I/O address identification.

b. Install the supplied threaded spacer on the solder side of the MULTIMODULE Board (at the hole near connector J1). Secure the spacer by hand-tightening one of the supplied 1/4-inch screws through the component side of the iSBX 217C board (refer to Figure 2-5).

c. Locate pin 1 on the host iSBX connector. Similarly, locate pin 1 on the iSBX 217C board iSBX connector. Refer to Figure 2-6.

d. Carefully match the connectors at pin 1 and insert the iSBX 217C board into the host board iSBX connector until it is fully inserted and correctly seated. The iSBX 217C board J1 connector should be oriented in the same direction as the host board's I/O connectors.

e. Push the remaining 1/4-inch screw up through the bottom of the host board and thread it into the spacer.

f. Tighten down both screws as shown in Figure 2-5.

g. Refer to Section 2.4 for jumper connection information. If jumper connections are not required, install the host board back into its chassis.

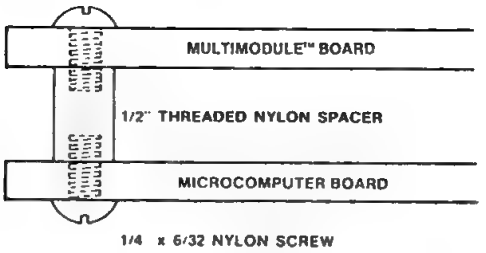

Figure 2-5. Mounting Technique

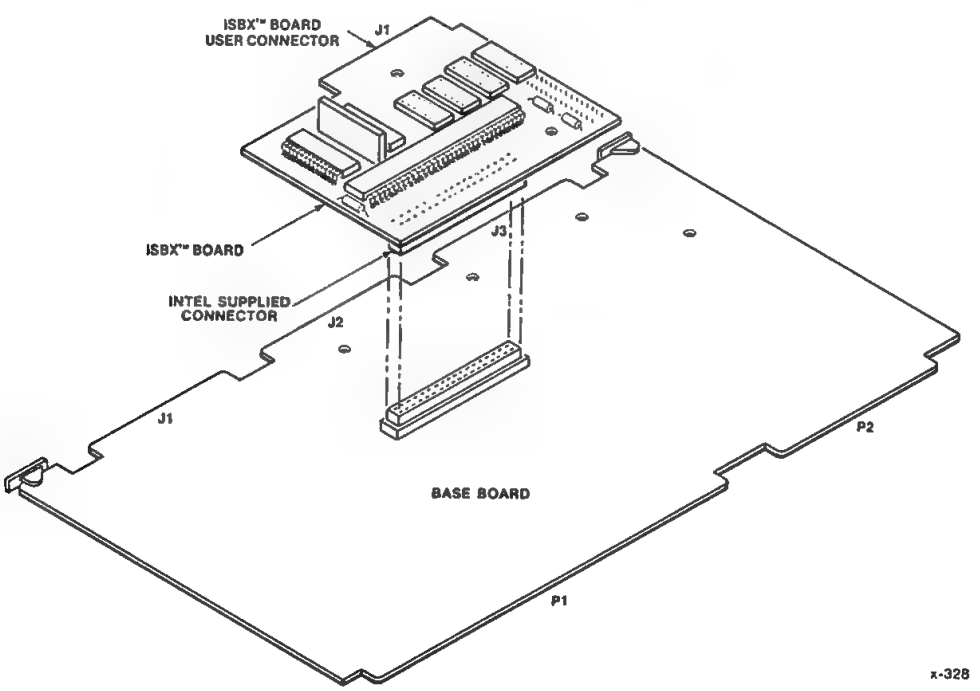

Figure 2-6. iSBX™ Board Installation

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CHAPTER 3
INTERFACING AND PROGRAMMING INFORMATION

3.1 INTRODUCTION

This chapter provides interfacing information and programming information for the iSBX 217C board. This information includes I/O addressing information, initialization information, command and command parameter instructions, host software requirements, and example flowcharts.

Throughout this chapter, abbreviations or mnemonics are used when referencing certain commands, status conditions, or common computer terms. The following table gives a brief definition of these abbreviations:

Mnemonic	Meaning in this Chapter
DMA:	Direct Memory Access.
EOT:	End Of Transfer (command).
IBF:	Input Buffer Full (status condition of UPI).
I/O:	Input/Output; here refers to mode of transfer.
OBF:	Output Buffer Full (status condition of UPI).
SOD:	Drive Ready (status of tape drive).
SOT:	Start Of Transfer (command).
UPI:	Universal Peripheral Interface (8742 microcomputer).
XFER:	Transfer (operation).

3.2 GENERAL OPERATION

There are four different operating modes in which the host and the iSBX 217C board communicate to transfer data to or from the tape drive:

a. Direct memory access (DMA) mode with QIC-Ø2 drive;

b. Programmed I/O mode with QIC-Ø2 drive;

c. DMA mode with 3M drive; and

d. Programmed I/O mode with 3M drive.

The difference between DMA and programmed I/O is illustrated by the behavior of the host board during the transfer. In general, the DMA mode requires that the host transfer a byte of data when the iSBX 217C board makes a DMA request. In the programmed I/O mode the host board polls a bit in the UPI (microcomputer on the iSBX 217C board) status register. When this bit becomes true the data can be transferred. Detailed

descriptions of the modes are in the following sections: QIC-Ø2 DMA, Section 3.5.1; QIC-Ø2 programmed I/O, Section 3.5.2; 3M DMA, Section 3.5.3; and 3M programmed I/O, Section 3.5.4.

A summary of commands is given in Section 3.3. Following the introduction to the commands, Sections 3.3.1 and 3.3.2 discuss the protocol for issuing commands. System operation is discussed in Section 3.5. Detailed descriptions of the commands are listed in Section 3.6.

3.3 COMMAND IMPLEMENTATION

A command must be given to the iSBX 217C board to initiate every function. Every command must be completed, i.e., the sense status bytes must be read (see Section 3.7), before a new command can be given. After a command is sent to the iSBX 217C board, the host may either poll the output buffer full (OBF) bit of the UPI, or be interrupted by MULTIMODULE interrupt Ø (MINTRØ) to signify the end of the function, before reading the sense status bytes.

All commands are followed by at least one parameter byte. Some of the commands can be used by both drive types; however, other commands are unique to one drive type only.

The iSBX 217C board utilizes three types of commands (see Table 3-1):

a. Simple Commands. These are commands which the host issues, and the iSBX 217C board executes the command and returns the status of the drive. Once the host issues a simple command, no further action is required except to receive the status. The receive status function includes waiting for the requested function to complete.

b. Data Transfer Commands. These commands cause data to be transferred to or from the tape. In this type of command the host issues the data transfer command, issues a special purpose command, transfers the data, issues a special purpose command, and receives the status. The data transfer command is not complete until the host receives the status.

c. Special Purpose Commands. These commands are used to synchronize the host and the iSBX 217C board during data transfers. A special purpose command can be issued ONLY during the execution of a data transfer command. The only special purpose command which returns status is the Reset Bad Parity Flag command.

Table 3-1 summarizes the complete command set. This table shows the hexadecimal code for the particular command, indicates the type of command (simple, data transfer, or special purpose), and indicates the number of parameter bytes required by the command.

The host issues commands to the iSBX 217C board by writing to specific host board I/O ports. In turn, the host reads UPI status and drive status through the same ports. Data is read or written through another set of ports. Addressing is described in more detail in Section 3.4.

Table 3-1. Command Set Summary

Hex Code	Command	Parameter Bytes		Type of Command
		QIC-Ø2	3M	
ØØ	RESET iSBX 217C BOARD	1	1	a
Ø1	INITIALIZE DRIVE	1	1	a
Ø2	WRITE A BLOCK	1	3	b
Ø3	WRITE A FILE MARK	1	1	a
Ø4	READ A BLOCK	1	3	b
Ø5	READ FILE MARK COMMAND	1	N	a
Ø6	READ STATUS	1	1	a
Ø7	REWIND	1	N	a
Ø8	RETENSION	1	N	a
Ø9	ERASE TAPE	1	N	a
ØC	UNLOAD TAPE	N	1	a
14	CONTINUE	N	1	a
15	WRITE RAM	N	5	b
16	READ RAM	N	5	b
17	VERIFY	N	5	a
18	RUN SELFTEST 1	1	N	a
1A	READ EXTENDED STATUS	1	N	a
1B	SET ALTERNATE SELECT MODE	1	N	a
1C	RETURN RAW DRIVE STATUS	1	N	a
2Ø	RESET BAD PARITY FLAG	Ø	N	c
4Ø	START OF TRANSFER (SOT)	1	1	c
8Ø	END OF TRANSFER (EOT)	1	1	c
81	PAUSE COMMAND	1	N	c
82	RELEASE PAUSE COMMAND	1	N	c

Notes: N = invalid command for drive; see text.
a = simple command
b = data transfer command
c = special purpose command
(See Section 3.3 for description of commands.)

3.3.1 PROTOCOL FOR ISSUING COMMANDS

The protocol for issuing commands from the host board to the iSBX 217C board is as follows:

1. Wait for IBF to be Ø.
2. Send command to iSBX 217C port.
3. Wait for IBF to be Ø.
4. Send 1st parameter to parameter port.
5. Wait for IBF if second parameter is required.
6. Send next parameter, if required (3M only).
7. Repeat steps 5 and 6 for remaining parameters (3M only).

Anytime the host board waits for IBF to be Ø it must also be able to detect the end of a function, either by MINTRØ or by polling OBF. If the end of the transfer is detected then the host board should skip the rest of the issuing command protocol and go on and receive the status.

3.3.2 PROTOCOL FOR RECEIVING STATUS

The protocol for receiving status from the iSBX 217C board is as follows:

1. Wait for OBF to be 1.
2. Read sense byte Ø.
3. Repeat steps 1 and 2 for the number of sense status bytes indicated in sense byte Ø (see Section 3.7).

3.4 I/O ADDRESSING

I/O port addresses vary with the particular host board in use. Table 3-2 summarizes the iSBX I/O port addresses for various host boards. To select Base Ø addresses, the signal MCSØ* must be true; to select Base 1 addresses, MCS1* must be true.

The host board iSBX board connector determines the range of addresses which must be used for host/iSBX dialog. Table 3-3 summarizes iSBX 217C command, data, and status addressing.

3.5 OPERATION

The host communicates with the iSBX 217C board in five basic ways to send commands, read or write data, and to check status. These ways are summarized as follows:

1. Host issues a simple command.
2. Programmed I/O read transfers.
3. Programmed I/O write transfers.
4. DMA read transfers.
5. DMA write transfers.

These five methods of operation are discussed in the following paragraphs. Notice that except for simple commands, the methods for the QIC-Ø2 drive are somewhat different than the methods for the 3M drive.

In a few remote cases, a breakdown in host-to-drive communication may develop, due to tape drive anomalies. Refer to Appendix A for a discussion of these drive anomalies.

Table 3-2. Selected iSBC® Board Connector Port Assignments for iSBX™ Boards

Board	DMA	iSBX Conn	CMD FUNCT/ UPI Status	CMD PARAM/ Drive Status	Data
iSBC 215G	Yes	J3	CØ72/6/A/E	CØ7Ø/4/8/C	CØBØ - CØBE+
		J4	CØD2/6/A/E	CØDØ/4/8/C	CØEØ - CØEE+
iSBC 589	Yes	J2	FF82/6/A/E	FF8Ø/4/8/C	FF9Ø - FF9F+
		J3	FFA2/6/A/E	FFAØ/4/8/C	FFBØ - FFBF+
iSBC 2Ø8	Yes	J3	21/3/5/7	2Ø/2/4/6	28 - 2F
iSBC 88/45	Yes	J4	C1/3/5/7	CØ/2/4/6	C8 - CF
		J5	F1/3/5/7	FØ/2/4/6	F8 - FF
iSBC 8Ø/1ØB	No	J4	F1/3/5/7	FØ/2/4/6	F8 - FF
iSBC 8Ø/16	No	J4	C1/3/5/7	CØ/2/4/6	C8 - CF
		J5	F1/3/5/7	FØ/2/4/6	F8 - FF
iSBC 8Ø/24	No	J5	C1/3/5/7	CØ/2/4/6	C8 - CF
		J6	F1/3/5/7	FØ/2/4/6	F8 - FF
iSBC 88/4Ø	No	J4	81/3/5/7	8Ø/2/4/6	9Ø - 9F+
		J5	A1/3/5/7	AØ/2/4/6	BØ - BF+
		J6	61/3/5/7	6Ø/2/4/6	7Ø - 7F+
iSBC 88/25	No	J3	81/3/5/7	8Ø/2/4/6	9Ø - 9F+
		J4	A1/3/5/7	AØ/2/4/6	BØ - BF+
iSBC 86/Ø5, iSBC 86/3Ø, iSBC 86/35	No	J3	A2/6/A/E	AØ/4/8/C	BØ - BF+
		J4	82/6/A/E	8Ø/4/8/C	9Ø - 9F+
iSBC 186/Ø3	No	J6	A2/6/A/E	AØ/4/8/C	BØ - BF+
		J7	82/6/A/E	8Ø/4/8/C	9Ø - 9F+
iSBC 286/1Ø	No	J5	A2/6/A/E	AØ/4/8/C	BØ - BF+
		J6	82/6/A/E	8Ø/4/8/C	9Ø - 9F+

Notes: + = Use EVEN addresses only for DATA column (i.e., BØ, B2, B4, B6, etc.).

All address are shown in hexadecimal. For CMD FUNCT and CMD PARAM, the addresses shown perform the same function. For example, on the iSBC 86/3Ø board using J4, reading or writing to port 8Ø is equivalent to reading or writing to port 84, 88, or 8C. For data transfers, any address in the range performs the data operation.

Table 3-3. iSBX™ 217C Board I/O Port Addressing

iSBX™ 217C Port Address	Port Function
Base Ø @ Ø, 2, 4, 6 (8-bit host) or Ø, 4, 8, C (16-bit host)	Write command parameter or read drive status
Base Ø @ 1, 3, 5, 7 (8-bit host) or 2, 6, A, E (16-bit host)	Write command function or read UPI status
Base + 1 @ Ø through 7 (8-bit host) or Ø through F EVEN only (16-bit host)	Write or read data

For simple commands, the command and parameters are sent to the UPI and then the status is returned. The host must be able to detect the end of the operation at anytime. The sequence for a simple command is:

1. Send simple command and its parameters to UPI.
2. Receive status.

The following four sections describe how to use the iSBX 217C board with each drive type. Both methods of transfer (DMA and Programmed I/O) are given. Figure 3-1A is a flowchart of a simple command. Figure 3-1B shows the recommended sequence for issuing the command byte. Figure 3-1C shows the sequence for issuing a parameter byte. Figure 3-2A shows a data transfer operation, and Figure 3-2B shows the method of reading the returned status sense bytes.

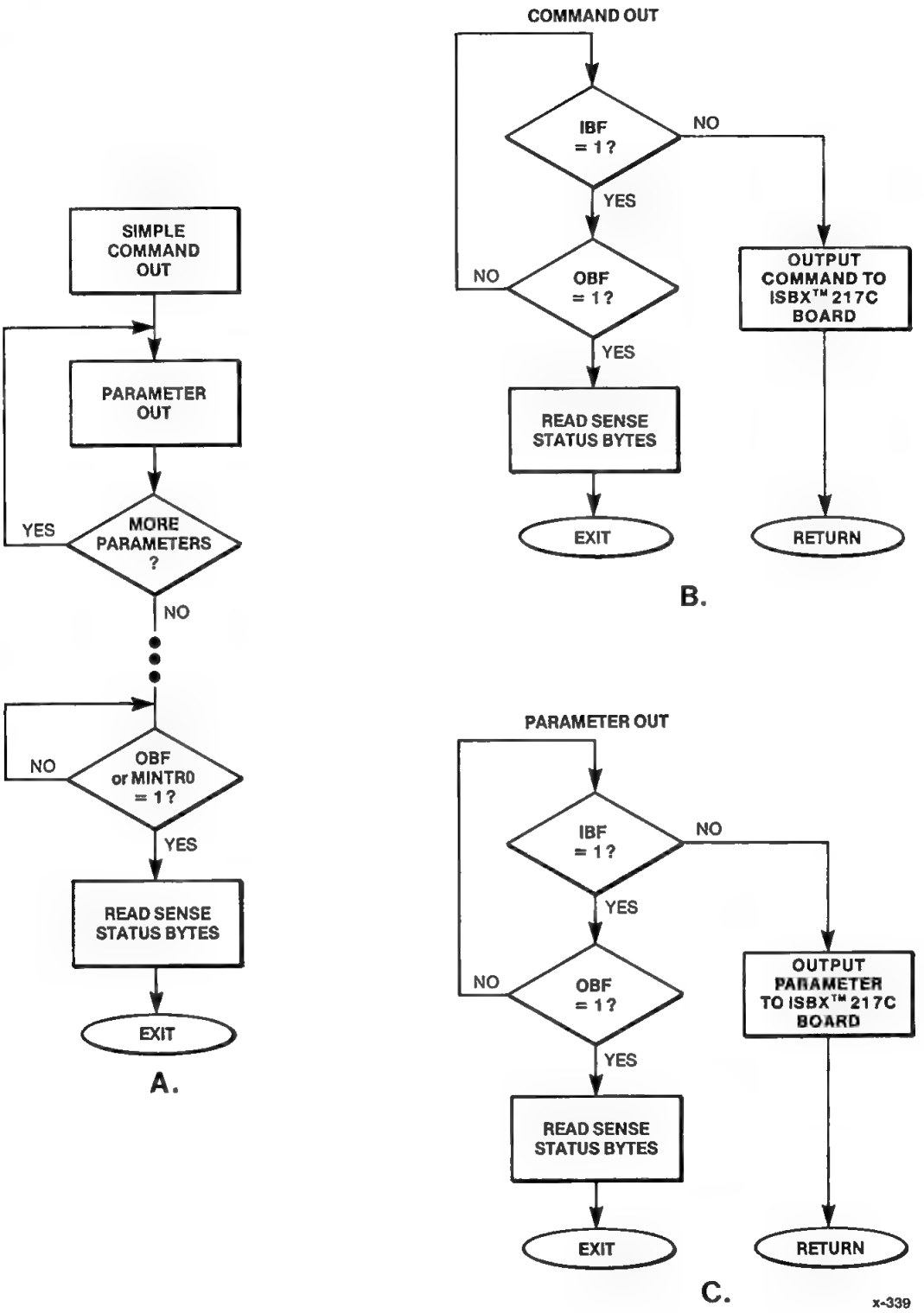


Figure 3-1. Example Flowcharts

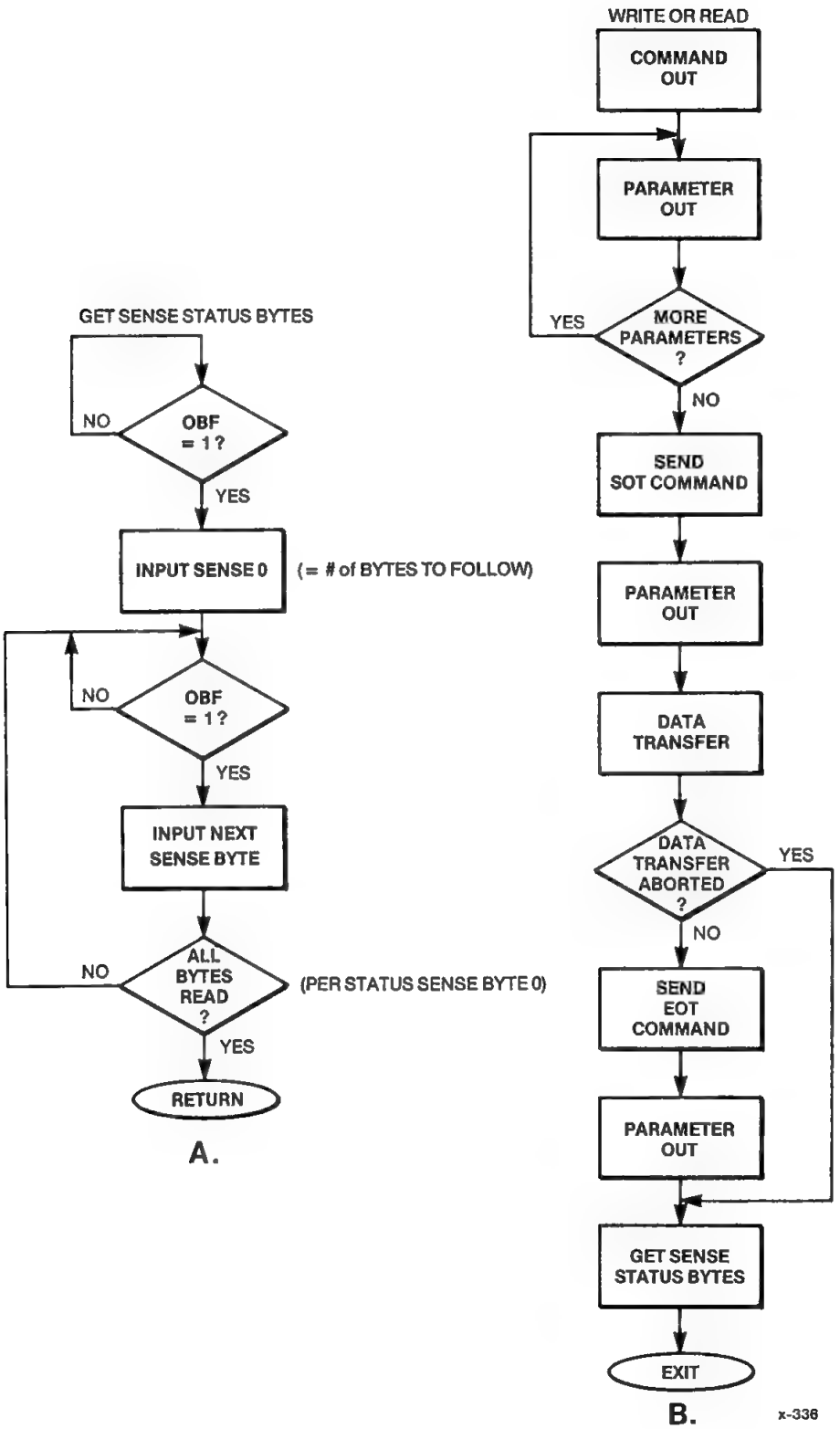


Figure 3-2. Example Flowcharts

3.5.1 QIC-02 DRIVE USING DMA MODE

Hosts that use Direct Memory Access (DMA) capability must use DMA request (DMRQT) to synchronize data transfer. However, the use of DMA acknowledge (MDACK*) is optional. For example, the iSBC 215G Winchester Disk Drive Controller board performs data transfer with no DMA acknowledge because in reality the iSBC 215G board executes a programmed I/O transfer with the iSBX 217C board while performing DMA transfers over the MULTIBUS system. Additionally, the DMA hardware must have the capability for an external termination (TDMA) so that in the event the drive has experienced an unrecoverable error, the iSBX 217C board can terminate operation.

The host should examine the DMA byte count register after completion of the transfer. If the full byte count has not been transferred, the drive terminated the operation and the host should examine the sense status bytes for any hard errors. Figure 3-3 shows a timing diagram of a DMA transfer with external termination caused by a hard data error.

The following procedure gives the DMA READ data transfer operation:

1. Send a read command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Transfer the data.
5. Check for Parity Flag. If set, issue RESET BAD PARITY FLAG command.
6. Send an EOT command to the UPI.
7. Receive sense status bytes from the UPI.

The following procedure gives the DMA WRITE data transfer operation:

1. Send a write command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Transfer the data.
5. Send an EOT command to the UPI.
6. Receive sense status bytes from UPI.

At anytime during either sequence the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6. DMA enable can be delayed until the end of sending the SOT command. However DMA must be enabled when the SOT command parameter is sent to the iSBX 217C board.

For hosts which have an 8Ø89 controller (such as the iSBC 215G board) the code should be similar to the following:

```
SEND WRITE COMMAND
SET UP
WAIT FOR IBF
SEND SOT COMMAND
WAIT FOR IBF
XFER                        ;ENABLE DMA
MOVBI 217C, PARAMETER       ;SEND SOT PARAMETER
```

Notice that the actual data transfer in this mode does not begin until after the iSBX 217C board receives the SOT parameter.

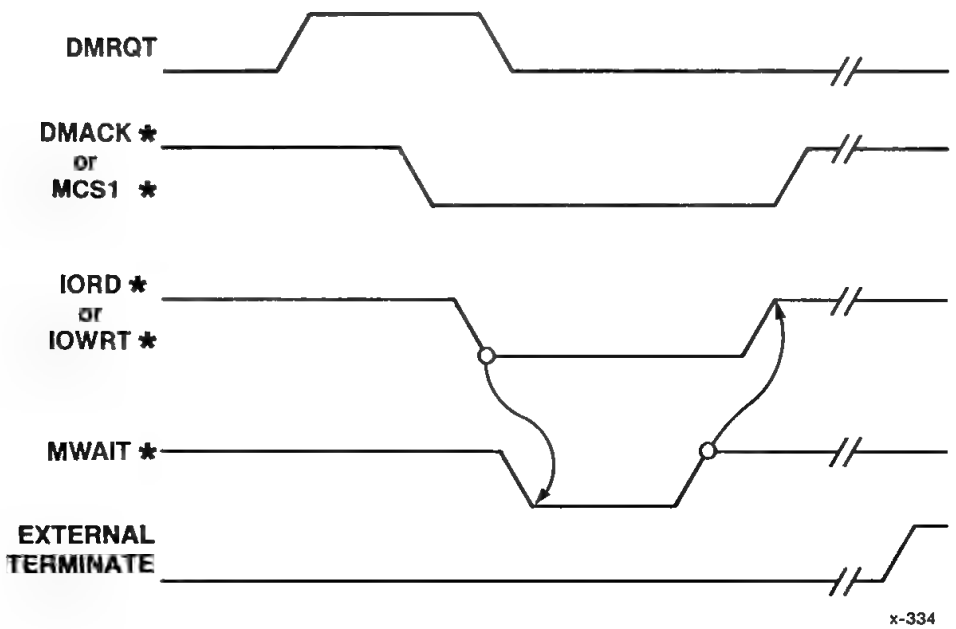


Figure 3-3. DMA Data Transfer Timing Diagram

3.5.2 QIC-02 DRIVE USING PROGRAMMED I/O MODE

For programmed I/O transfers, the host board must support the MWAIT* line on the iSBX bus. As soon as the host has given the command sequence to the iSBX 217C board, the data transfer for a read or write function can begin.

The host board must employ a high-speed programmed I/O loop, with the loop speed controlled by MWAIT*. Figure 3-4 depicts the sequence of events for write operation only. Figure 3-5 depicts the sequence of events for read operation only. For a read or write operation, when the host board accesses (Base 1), MWAIT* will go active if either the next data byte is not available for a read operation or if the drive is not ready to receive a byte for a write operation. As long as MWAIT* is active, the host board executes wait states. When the drive is ready for data, MWAIT* becomes inactive thereby permitting instruction execution to continue. Figure 3-6 is a timing diagram of this sequence.

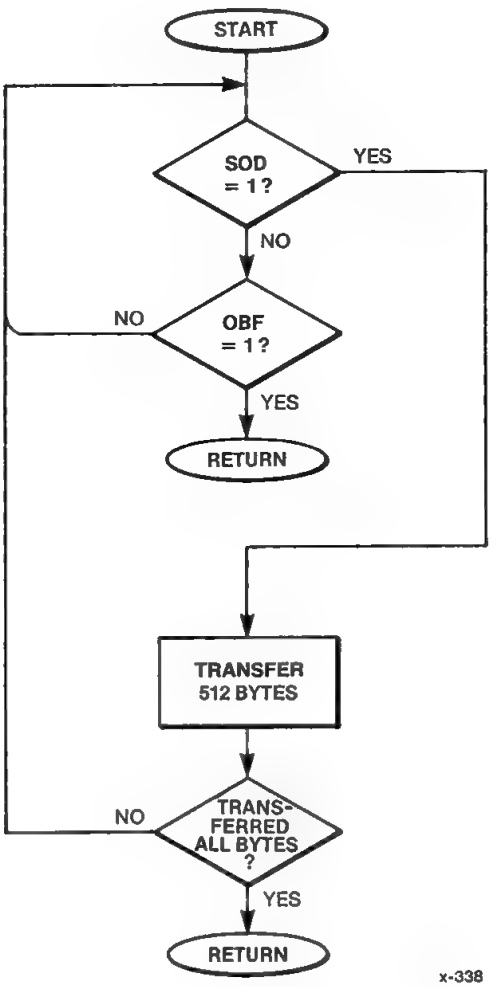


Figure 3-4. QIC-Ø2 Drive Programmed I/O Simplified Flow (Write Only)

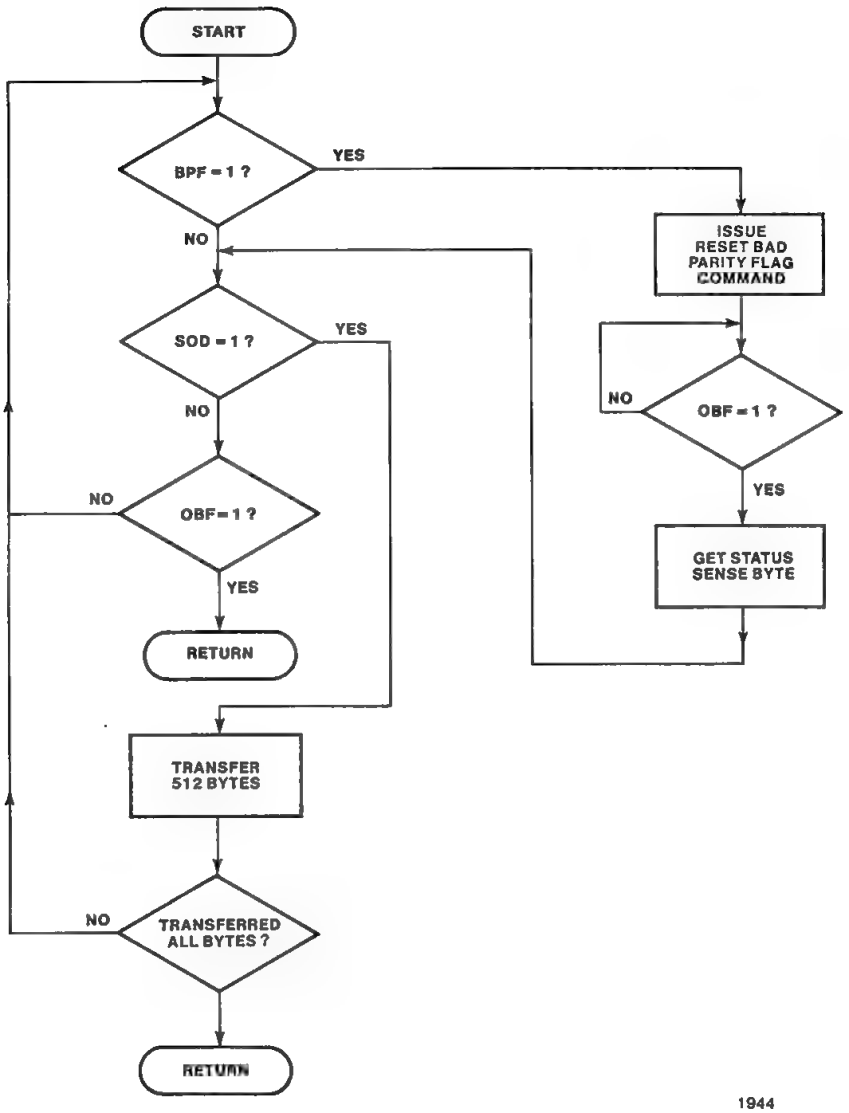


Figure 3-5. QIC-Ø2 Drive Programmed I/O Simplified Flow (Read Only)

In the event that a hard error prevents function completion, the iSBX 217C board sets OBF notifying the host that an error exists. The host board should then poll OBF and read the drive sense status bytes (see Section 3.7) to determine the type of error.

The host is required to transfer the data to and from the QIC-Ø2 drive at a rate greater than 1ØØK bytes/sec, or 3ØK bytes/sec, depending on the drive speed.

For the QIC-Ø2 interface at 9Ø ips operation, the host must read/write a byte to the drive every 11 microseconds or less. To attain that speed, the program loop should transfer data as fast as possible by synchronizing the iSBX transfers with MWAIT*.

Since the QIC-Ø2 drive has three 512 byte FIFO (first-in-first-out) buffers, the drive will always transfer data in blocks of 512 bytes. Therefore, it is the responsibility of the host to stop after every 512 data bytes are transferred and wait until another buffer is ready to be serviced.

The mechanism for checking for a buffer ready is for the host to poll the UPI status port. The bit definitions for the status port are as follows:

MSB	7	6	5	4	3	2	1	Ø	LSB

BØ: Output Buffer Full (OBF) - set to a logical one when the UPI writes to the data bus buffer. This bit is cleared when the host processor reads the data bus buffer.

B1: Input Buffer Full (IBF) - when a logical one, indicates the host has written a byte to the data bus buffer, and that the iSBX 217C board has not emptied the buffer.

B2-B4: Bits 2 through bits 4 are reserved.

B5: Pause Flag - when a logical one, indicates the host has issued a PAUSE command to the iSBX 217C board which then goes into an idle condition. This bit is cleared when the host board issues the RELEASE PAUSE command to the iSBX 217C board.

B6: Bad Parity Flag (BPF) - When the iSBX 217C board detects that a parity error has occurred during a data read transfer from the drive, this bit is set. To reset this flag, the RESET BAD PARITY FLAG command (2ØH) must be issued to the iSBX 217C board before terminating the read data transfer with the EOT command. If the data transfer is aborted by the drive, this flag is automatically reset by the iSBX 217C board.

B7: Buffer Ready (SOD) - when using an QIC-Ø2 interface with programmed I/O Control, this bit when = logical 1 tells the host that another 512 byte data block is ready to be transferred. The host should poll this bit for every block of data transferred.

If an unrecoverable error occurs, the iSBX 217C board sets MINTRØ active, and the host should poll OBF and read the sense status bytes until all are read.

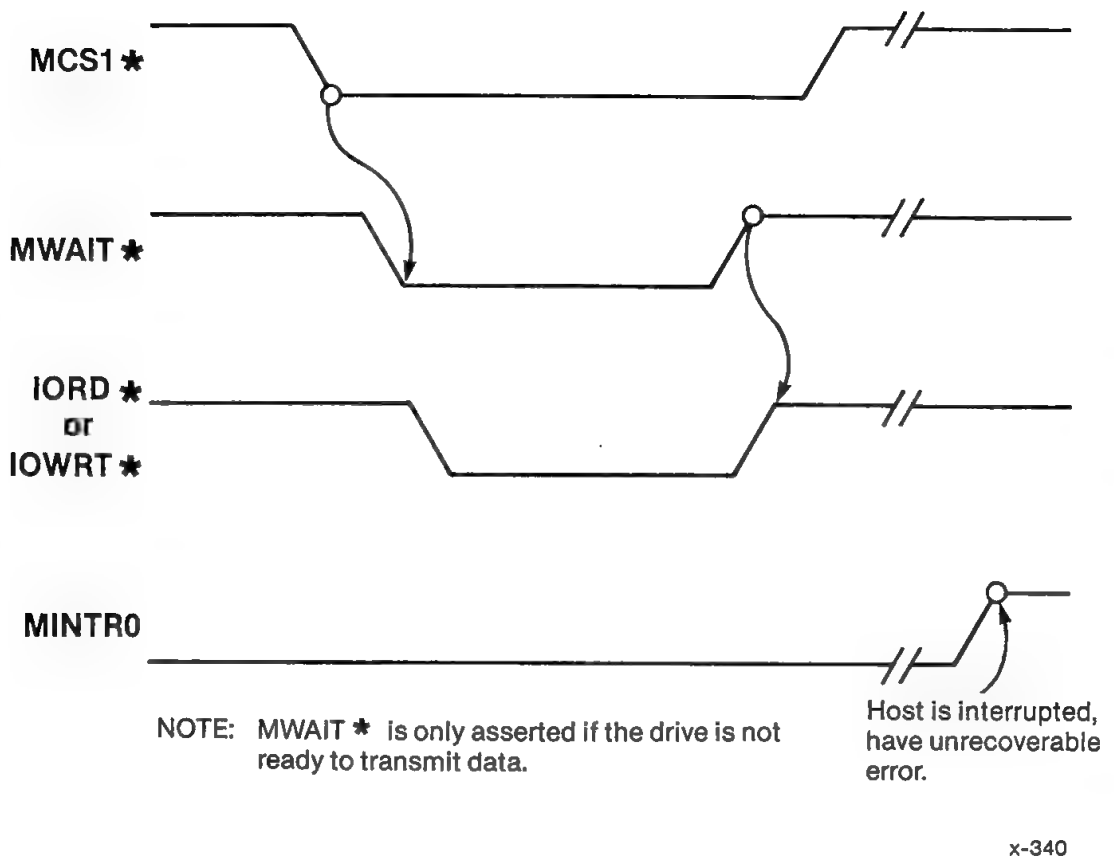


Figure 3-6. Programmed I/O Transfer Timing Diagram

If the host board does not support MINTRØ, the software can poll OBF and SOD at the data block boundary. If OBF = 1, this indicates (to the host) that the transfer was aborted and that the status sense bytes are ready to be read.

The reason the buffer ready must be polled every 512 bytes, is that letting the host run free could cause MWAIT* to be active for seconds, which could seriously degrade system performance and because most processor boards that produce a timeout interrupt when the wait line is active too long.

The following paragraphs summarize the procedure for the QIC-Ø2 drive. Remember that all QIC-Ø2 drive data transfers must be in multiples of 512 bytes. Figure 3-7 is a detailed flowchart of the QIC-Ø2 drive programmed I/O mode READ operation. Table 3-4 is the corresponding assembly language program for this operation.

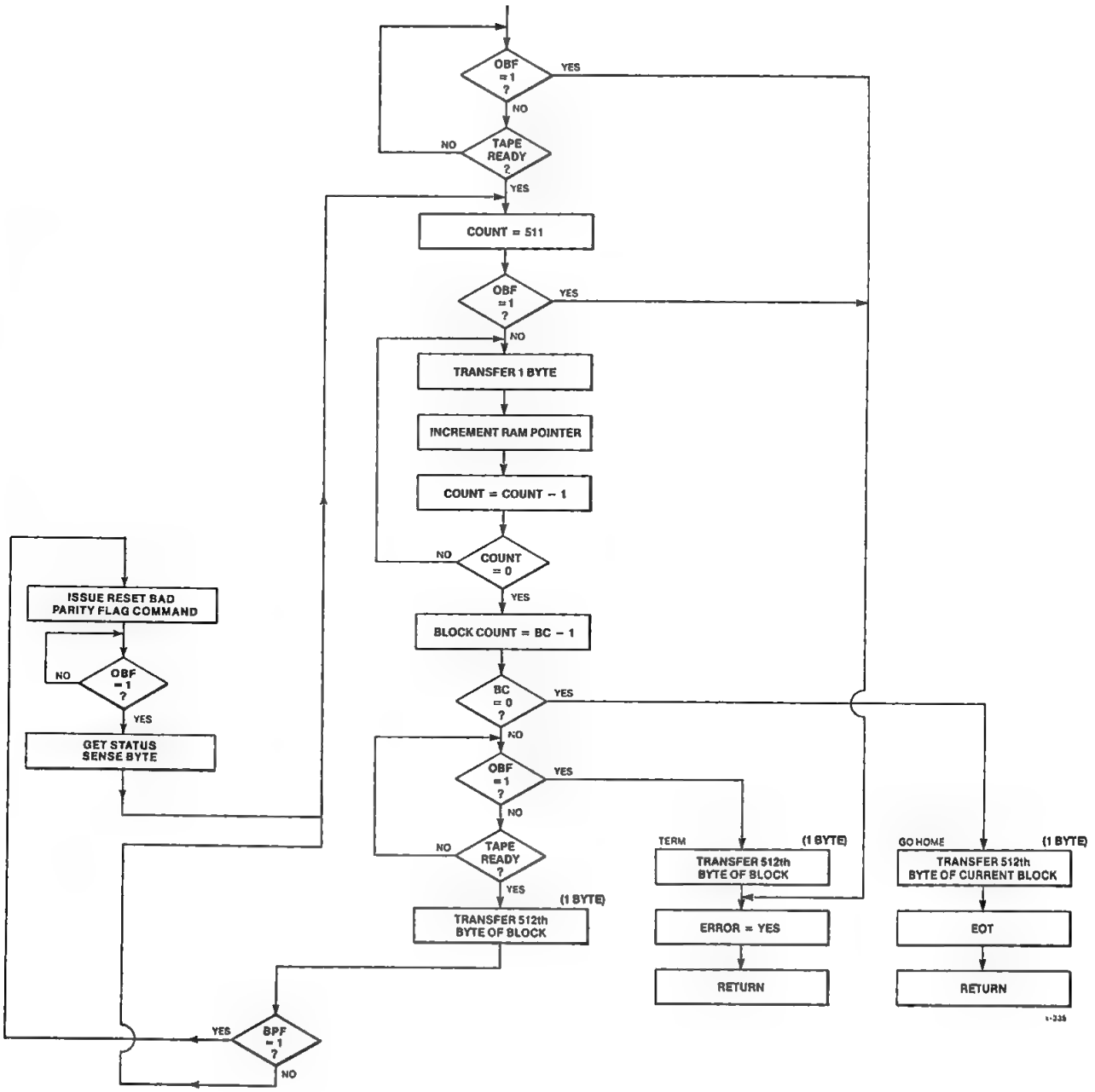


Figure 3-7. QIC-Ø2 Drive Detailed I/O Operation

Table 3-4. Program Example of QIC-Ø2 READ Operation

```
NAME        QUICK_TRANSFER
CGROUP        GROUP        CODE

EXTRN  BYTCOUNT:WORD
EXTRN  BLOCKCOUNT:WORD
EXTRN  BUF_PTR:DWORD
EXTRN  XFER$ERR:BYTE
EXTRN  LASTBYTE:BYTE

PUBLIC  IN_XFER
PUBLIC  OUT_XFER
PUBLIC  RD_XFER
PUBLIC  WR_XFER
PUBLIC  DMA_OK
PUBLIC  READ_QIC02_IO
PUBLIC  WRITE_QIC02_IO

UPI_STATUS       EQU        082H
COMMAND_217      EQU        082H
PARAM_217        EQU        080H
STATUS_37        EQU        088H
DATA_217         EQU        090H
OBF_MASK         EQU        01H
IBF_MASK         EQU        02H
TC_MASK          EQU        08H
READY_MASK       EQU        80H
END_XFER_217     EQU        80H
DMA0_COUNT_REG   EQU        0FFC8H
RBPLC            EQU        020H
BPL_MASK         EQU        040H

ASSUME        CS:CGROUP
CODE         SEGMENT WORD        PUBLIC        'CODE'

;********************** Reset Parity Error Bit *******************************

RBPLB       PROC    NEAR                ;ISSUES RESET PARITY BIT COMMAND
            MOV     AL,RBPLC            ;GET RESET COMMAND
            OUT     COMMAND_217,AL      ;ISSUE COMMAND
@0003:      IN      AL,UPI_STATUS       ;WAIT FOR PARAMETER BYTE
            AND     AL,OBF_MASK
            JZ      @0003
            IN      AL,PARAM_217
            RET
RBPLB       ENDP

;********************** INCREMENT SEGMENT REGISTER ****************************

UPSEG       PROC    NEAR                ;INCREMENTS SEGMENT REGISTER, ES
            PUSH    ES
            POP     CX
            ADD     CX,1000H
            PUSH    CX
            POP     ES
            RET
UPSEG       ENDP
```

Table 3-4. Program Example of QIC-Ø2 READ Operation (continued)

```
;************************ READY TEST, XFER 512th ********************************
; SUBROUTINE TO CHECK READY AND READ 512th BYTE OF BLOCK

READY:      IN      AL,UPI_STATUS
            RCR     AL,1
            JC      LAST
            IN      AL,UPI_STATUS       ;CHECK FOR PARITY ERROR
            AND     AL,BPL_MASK         ;
            JZ      @0020               ;
            CALL    RBPLB               ;
@0020:      IN      AL,UPI_STATUS       ;CHECK READY AND
            AND     AL,READY_MASK       ;
            JZ      READY               ;
            IN      AL,DATA_217         ;READ 512th BYTE OF BLOCK
            MOV     ES:[SI],AL
            INC     SI
            JMP     RERET
LAST:       JMP     LAST1

;************************ QIC02 I/O READ TRANSFER ****************************
; XFERS BYTCOUNT FROM TAPE TO RAM @ BUF_PTR

READ_QIC02_IO     PROC    NEAR
IBFLKR:     IN      AL,UPI_STATUS       ;WAIT ON IBF                    ^
            AND     AL,IBF_MASK         ;                               |
            JNZ     IBFLKR              ;                               |
OBFLKR:     IN      AL,UPI_STATUS       ;CHECK FOR OBF TERMINATION      |
            RCR     AL,1                ;                          < Initialize >
            JC      HURTR               ;                               |
            IN      AL,UPI_STATUS       ;CHECK FOR PARITY ERROR         |
            AND     AL,BPL_MASK         ;                               |
            JZ      @0001               ;                               |
            CALL    RBPLB               ;                               |
@0001:      IN      AL,UPI_STATUS       ;WAIT FOR TAPE READY            |
            AND     AL,READY_MASK       ;                               |
            JZ      OBFLKR              ;                               |
            LES     SI,DS:BUF_PTR       ;INDEX TO RAM                   V
FRESHR:     MOV     CX,511              ;INNER "LOOP" COUNTER           ^
            IN      AL,UPI_STATUS       ;CHECK FOR OBF TERMINATION      |
            RCR     AL,1                ;                               |
            JC      HURTR               ;                               |
TIGHTR:     IN      AL,DATA_217         ;READ FROM TAPE       <Xfer 511 bytes>
            MOV     ES:[SI],AL          ;WRITE TO RAM                   |
            INC     SI                  ;                               |
            LOOP    TIGHTR              ;                               V
            DEC     DS:BLOCKCOUNT       ;CHECK FOR ALL DONE (-1),       ^
            JZ      HOMER               ;IF SO GRAB LAST AND GO.        |
            IN      AL,UPI_STATUS       ;CHECK FOR DRIVE EXCEPTION      |
            RCR     AL,1                ;                               |
            JNC     NOOBFR              ;                               |
LAST1:      IN      AL,DATA_217         ;IF EXCEPTION (OBF) THEN        |
            MOV     ES:[SI],AL          ;GRAB LAST AND BAIL OUT,        |
            JMP     HURTR               ;                    <Done,obf or loop? >
NOOBFR:     JMP     READY               ;ELSE GRAB 512th AND LOOP.      |
RERET:      CMP     SI,0                ;CHECK FOR INDEX OVERRUN        |
            JNZ     FRESHR              ;                               |
            CALL    UPSEG               ;INCREMENT THE SEGMENT REGISTER
            JMP     FRESHR              ;                               V
HOMER:      IN      AL,DATA_217         ;512th OF LAST BLOCK            ^
            MOV     ES:[SI],AL          ;                               |
            MOV     CS,80H              ;SET UP TIMING LOOP TO LET UPI GET LAST
TIMR01:     LOOP    TIMR01              ;BYTE PARITY CHECKED AND FLAGGED.
            IN      AL,UPI_STATUS       ;CHECK FOR PARITY ERROR         |
            AND     AL,BPL_MASK         ;                               |
            JZ      @0010               ;                               |
            CALL    RBPLB               ;                               |
@0010:      MOV     AL,END_XFER_217     ;                               |
            OUT     COMMAND_217,AL      ;                               |
IBFPR:      IN      AL,UPI_STATUS       ;                               |
            AND     AL,IBF_MASK         ;            < 512th byte,EOT and return >
            JNZ     IBFPR               ;                               |
            MOV     AL,0                ;                               |
            OUT     PARAM_217,AL        ;                               |
            RET                         ;                               V
HURTR:      MOV     AL,0FFH             ;BAIL OUT POINT FROM AN EXCEPTION
            MOV     DS:XFERSERR,AL
            RET
READ_QIC02_IO     ENDP

CODE        ENDS
            END
```

3.5.2.1 QIC–02 Drive READ Procedure In Programmed I/O Mode

The host board sequence for performing a READ operation is:

1. Send a READ command TO THE UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data. See method below.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

The method of checking for a buffer ready condition at the 512 byte boundary during a READ operation is as follows:

1. Transfer 511 bytes;
2. If more blocks are to follow, then wait for buffer ready; else go to step 6;
3. Transfer 1 byte;
4. Check for Bad Parity Flag. If set, issue RESET BAD PARITY FLAG command.
5. Go to step 1;
6. Transfer 1 byte;
7. Done.

At anytime during this sequence the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6.

The purpose of the SOD bit is to prevent the host board from executing wait states for long periods of time while the drive searches for the next block. If the host board follows this SOD protocol, and performs the I/O transfer synchronized on DMA request (DMACK), the firmware ensures that the host board does not execute wait states for more than 1 millisecond.

CAUTION

Before issuing the EOT command to the iSBX 217C board, the Bad Parity Flag in the UPI Status Register must be checked. If the flag indicates bad parity, the RESET BAD PARITY FLAG command must be issued to the iSBX 217C board. Failure to issue the RESET BAD PARITY FLAG command (at this point) will cause a drive fault to be indicated in the sense bytes returned to the host board.

3.5.2.2 QIC-02 Drive WRITE Procedure In Programmed I/O Mode

The host board sequence for performing a WRITE operation is:

1. Send a WRITE command to the UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data. See method below.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

At anytime during this sequence the host board must be able to perceive the end of the operation. If the end of the operation is perceived before the host board has reached step 6, the host should go directly to step 6.

NOTE

If the drive detects a write parity error, it aborts the transfer and the parity error is indicated in the sense bytes.

The method of checking for a buffer ready condition at the 512 byte boundary for a WRITE operation is as follows:

1. Transfer 512 bytes;
2. If more blocks are to follow, then wait for buffer ready; else go to step 4;
3. Go to step 1;
4. Done.

3.5.3 3M DRIVE USING DMA

The host board sequence for performing a DMA READ operation is as follows:

1. Send a read command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Wait for data transfer to complete.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

The following procedure gives the DMA WRITE data transfer operation:

1. Send a write command to the UPI.
2. Set up DMA hardware and enable.
3. Send a SOT command to the UPI.
4. Wait for data transfer to complete.
5. Send an EOT command to the UPI.
6. Receive status from UPI.

At anytime during either sequence the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6. DMA enable can be delayed until the end of sending the SOT command. However DMA must be enabled when the SOT command parameter is sent to the iSBX 217C board.

For hosts which have an 8Ø89 controller (such as the iSBC 215G board) the code should be similar to the following:

```
SEND WRITE COMMAND
SET UP
WAIT FOR IBF
SEND SOT COMMAND
WAIT FOR IBF
XFER                        ;ENABLE DMA
MOVBI 217C, PARAMETER       ;SEND SOT PARAMETER
```

Notice that the actual data transfer in this mode does not begin until after the iSBX 217C board receives the SOT parameter.

3.5.4 3M DRIVE USING PROGRAMMED I/O

The programmed I/O sequence is different for the 3M interface because the HCD-75 interface does not indicate when the next buffer is available. However, because the transfer rate of the drive is only 17.5K bytes/second, the data transfer could be interrupt-driven on a byte-by-byte basis using iSBX Option Line 1 tied to an interrupt input.

Alternatively, this line could be connected to the host board's parallel port and polled. Option line 1 is tied to MDRQT (DMA request). When this line is active (high) it indicates that the host can transfer the next data byte to or from the iSBX 217C board.

Another method could be employed by disabling the timeout on the host board, and then synchronizing the transfers with MWAIT.

The buffer ready bit (SOD) is set for the first ready buffer and stays set for the duration of the transfer. The host must not start the transfer until SOD is a 1.

The following procedure summarizes the routines for the 3M drive. All 3M drive data transfers must be in multiples of 2 bytes; this is a restriction placed on the system by the drive. Figure 3-8 is a flowchart of the read/write process on the 3M drive using OPT1 to synchronize data transfers.

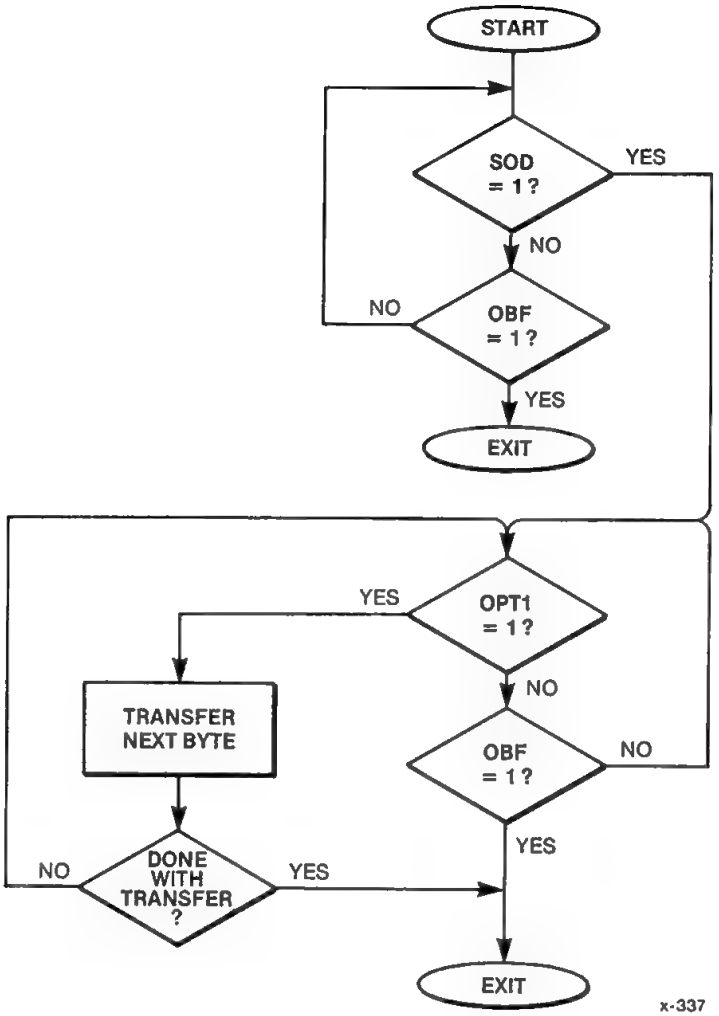


Figure 3-8. 3M Drive Programmed I/O Data Transfer

The host board sequence for performing a READ operation is:

1. Send a READ command TO THE UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

The host board sequence for performing a WRITE operation is:

1. Send a WRITE command to the UPI.
2. Send a SOT command to the UPI.
3. Wait for SOD bit in UPI status.
4. Transfer the data.
5. Send an EOT command to the UPI.
6. Receive status from the UPI.

At anytime during either a READ or a WRITE operation the host board must be able to perceive the end of the operation. If the end to the operation is perceived before the host board has reached step 6, the host should go directly to step 6.

Note that if the READ programmed I/O operation using MWAIT* terminates before the host has finished transferring the data, the host reads an extra byte. Therefore, the host software must be able to handle this type of termination.

3.6 COMMAND DESCRIPTIONS

All on-board functions are controlled by firmware contained in the UPI device on the iSBX 217C board. The two supported tape drive interfaces (QIC-Ø2 & 3M) do not require an identical number of commands. However, the iSBX 217C board supports all required commands for each drive interface. Table 3-1 summarizes the commands available on the iSBX 217C board. The table indicates whether the interface supports a particular iSBX 217C board command and if so, the table indicates the number of parameter bytes that are required with the command. The hexadecimal value for each command is also shown.

Each command is initiated by writing the specified command code to the UPI command port, followed by at least one parameter byte transferred via the UPI data port.

For every command initiated, the host must read the sense status bytes at the conclusion of that operation. The exceptions are Read, Write, and SOT commands, where the sense status bytes are automatically returned to the host after the End of Transfer command is sent. If the iSBX 217C board terminates the command, the sense status bytes are returned to the host without the EOT command.

The host can either poll the OBF (Output Buffer Full) flag in the UPI status port or the host can be interrupted by MINTRØ when the drive sense status bytes require reading by the host. MINTRØ stays set until the UPI reads the first sense status byte. The host must poll OBF for the remaining sense status bytes. Every command has at least one parameter byte, called parameter byte Ø (Figure 3-9).

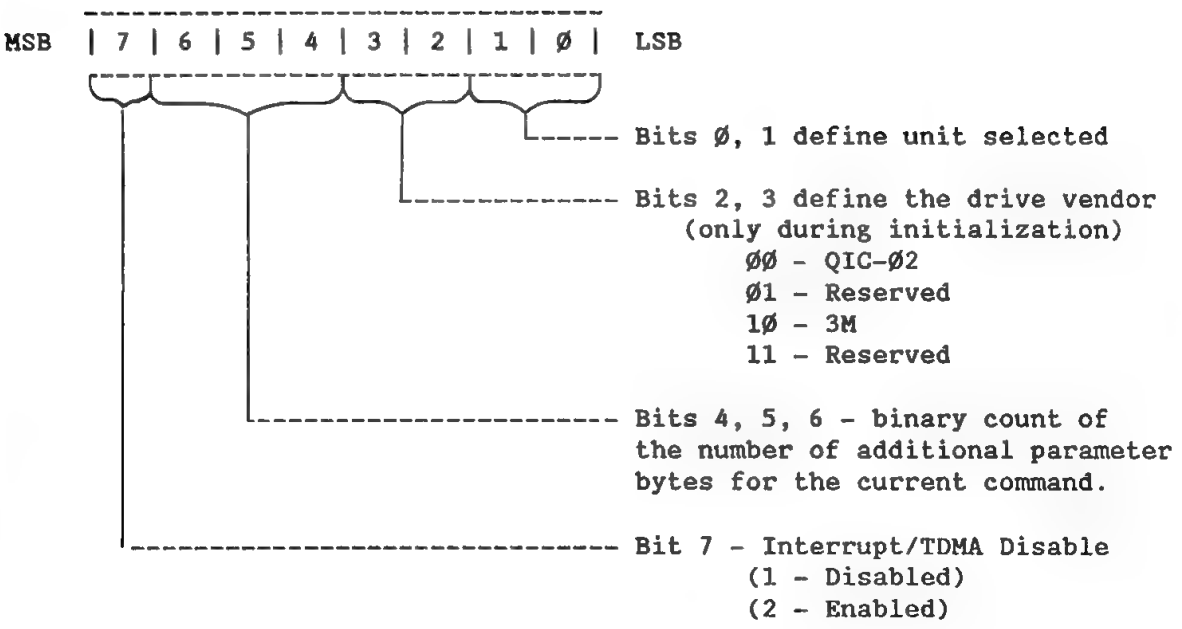


Figure 3-9. Parameter Byte Ø

The host board must issue a Start of Transfer (SOT) command to the iSBX 217C board before starting the data transfer (WRITE or READ), and an End of Transfer command (EOT) once the data transfer is over. Optionally, the host board can issue the; PAUSE, RELEASE PAUSE and the RESET BAD PARITY FLAG commands to the iSBX 217C board during a data transfer command (READ or WRITE).

If, however, the iSBX 217C board aborts the transfer, the End of Transfer command is not required. The host should instead read the sense status bytes. The following 17 subsections describe the commands available on the iSBX 217C board. The commands are listed in numerical order. Unless otherwise indicated each 3M drive command requires only one parameter byte (all QIC-Ø2 drive commands require a maximum of one parameter byte).

3.6.1 SOFTWARE RESET COMMAND (00H)

PARAMETER BYTES: 1

This command causes the iSBX 217C board to perform a checksum test on its internal ROM and to clear its internal RAM. The RESET command also initializes control port P2. The Reset command must be given as the first command after power-up. The iSBX 217C board considers all other commands invalid until the RESET command has been issued. Once the RESET command has been issued, the iSBX 217C board accepts RESET or INITIALIZATION commands only. The drive not ready bit in the sense status byte is set at the completion of the RESET command.

3.6.2 INITIALIZATION COMMAND (01H)

PARAMETER BYTES: 1

The INITIALIZATION command must be the second command given after power-up and/or the RESET command. The INITIALIZATION command checks to see if the drive is present, resets the drive, and reads the drive status. Additionally, this command informs the iSBX 217C board which type of drive (QIC-Ø2 or 3M) is attached. Following initialization, the iSBX 217C board can accept any command which the attached drive supports. Figure 3-9 shows the format of the INITIALIZATION command parameter byte.

3.6.3 WRITE COMMAND (02H)

The behavior of this command depends on the drive type attached.

QIC-Ø2 Drive: PARAMETER BYTES: 1

The WRITE command writes a block of user data to the drive. For the QIC-Ø2 interface, the length of the block of data written to the drive can be any size as long as the byte count is in multiples of 512 bytes. Zeros must be appended at the end of the block if needed. Refer to the QIC-Ø2 specification for suggested data block lengths. The iSBX 217C board automatically writes a file mark on the tape after the host terminates the write function via the End of Transfer command (QIC-Ø2 interface only). The host may then issue another WRITE command and write another file.

3M Drive: PARAMETER BYTES: 3

For the 3M interface, data is stored on a pre-formatted tape with 1Ø24 bytes per block. The host is not required to write blocks of data in 1Ø24 byte increments, but is required to write an even number of bytes. The host must also supply the iSBX 217C board with starting block and track number (specified in parameter bytes 1 and 2). Figure 3-1Ø shows the format of the 2 parameter bytes.

3.6.4 WRITE FILE MARK COMMAND (03H)

The behavior of this command depends on the drive type attached.

The WRITE FILE MARK command is used to logically group data together by placing a filemark after the preceding data. One of the reasons for separating data into smaller segments is to prevent an unrecoverable loss of large data files.

QIC-Ø2 Drive: PARAMETER BYTES: 1

In the QIC-Ø2 interface only, the WRITE FILE MARK command is automatically issued at the conclusion of a WRITE command. Therefore, if the host issues another such command when interfaced to the QIC-Ø2 drive, a double file mark would be written on the tape.

3M Drive: PARAMETER BYTES: 1

In the 3M interface, the WRITE FILE MARK command writes an End Of File mark on the tape. This action uses the same amount of tape as a block of data.

3.6.5 READ COMMAND (04H)

The behavior of this command depends on the drive type attached.

The READ command reads a block of data from the drive. Both drive interfaces terminate the READ command when a file mark is detected.

QIC-Ø2 Drive: PARAMETER BYTES: 1

In the QIC-Ø2 interface, if the host does not read a whole file, i.e. detect a file mark, then at the completion of the End of Transfer, the tape will automatically rewind to the beginning of the tape. However, if a file mark is detected from the drive status bytes, then the host can issue another READ command and read the next file. As in the WRITE command, data must be transferred in 512 byte blocks. In the I/O read mode however, the tape ready bit (SOD) is polled between byte 511 and 512 of the block if using programmed I/O operation.

3M Drive: PARAMETER BYTES: 3

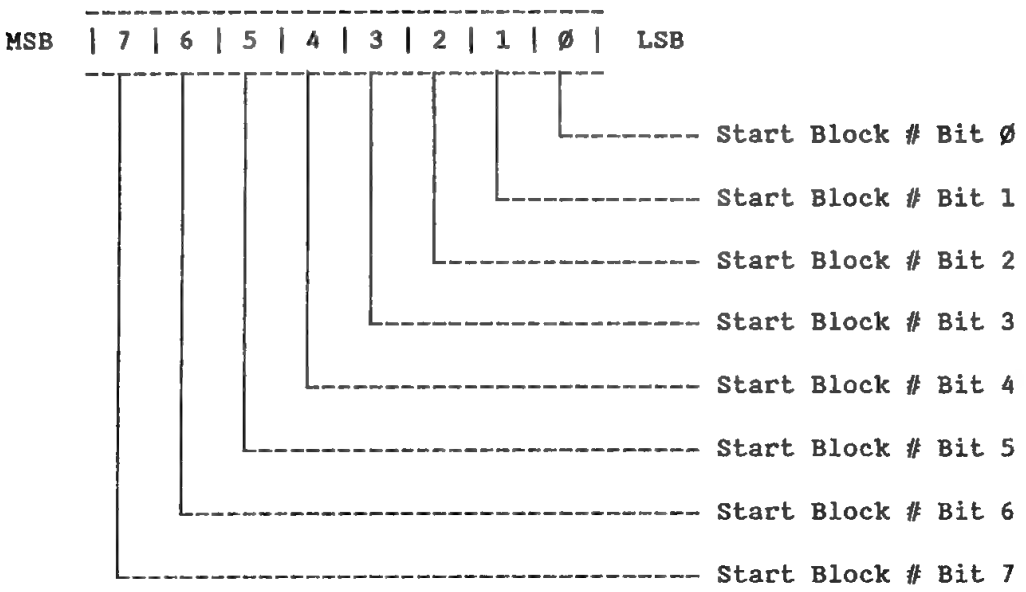
In the 3M interface, the READ function requires a block and track number with the same format as the WRITE command. Refer to Figure 3-1Ø. The host is not required to read the entire file; however, it must read an even number of bytes.

3.6.6 READ FILE MARK COMMAND (05H) - QIC-02 ONLY PARAMETER BYTES: 1

This command works in conjunction with the QIC-Ø2 interface only. It allows the host to count file marks without transferring any data. This command allows you to position the tape to the desired file. Following the command, the tape is positioned after the next file mark.

READ, WRITE COMMANDS

PARAMETER BYTE 1:



READ, WRITE COMMANDS

PARAMETER BYTE 2:

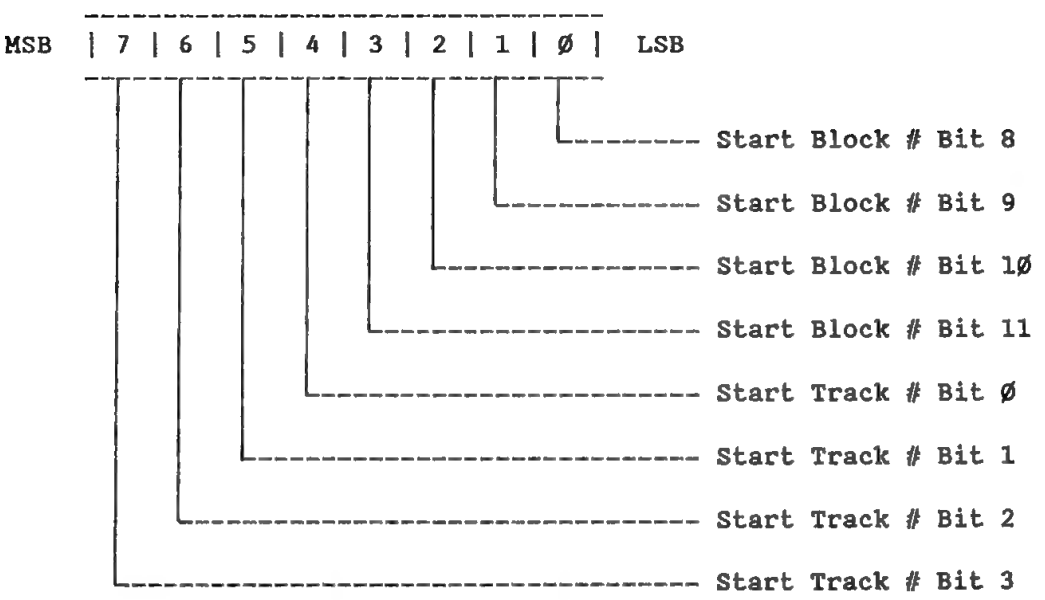


Figure 3-1Ø. Parameter Bytes 1 and 2 for READ/WRITE/VERIFY Commands (3M Drive Only)

3.6.7 READ STATUS COMMAND (06H) PARAMETER BYTES: 1

This command reads the status of the drive. Refer to Section 3.7 for additional drive status information.

3.6.8 REWIND COMMAND (07H) - QIC-02 DRIVE ONLY PARAMETER BYTES: 1

This command rewinds the tape to the beginning of the tape. This command should be issued after the INITIALIZATION command. This command must also be issued prior to changing the unit number (if more than one drive is attached).

3.6.9 RETENSION COMMAND (08H) - QIC-02 DRIVE ONLY PARAMETER BYTES: 1

The RETENSION command winds the tape from beginning to end and back to the beginning. This is done to equalize the tension throughout the tape.

3.6.10 ERASE TAPE COMMAND (09H) - QIC-02 DRIVE ONLY PARAMETER BYTES: 1

Used for the QIC-Ø2 interface only, this command should be used when the host is ready to use a new tape or re-recording on a used tape. If the host is to use the No Data Detect bit in the sense status bytes to find where the recorded data on the tape ends, the tape must be completely erased.

3.6.11 UNLOAD TAPE COMMAND (0CH) - 3M DRIVE ONLY PARAMETER BYTES: 1

Used for the 3M interface only, this command causes the cartridge to be wound to end of the tape. The Unload Tape command also unlocks the cartridge eject lever.

3.6.12 CONTINUE COMMAND (14H) - 3M DRIVE ONLY PARAMETER BYTES: 1

Used for the 3M interface only, the CONTINUE command causes the write operation to continue in the next block after an unreadable header is detected. After a READ command was terminated by a file mark, a Continue command will resume the READ command.

NOTE

The CONTINUE command should be used ONLY under the conditions described in Section 3.6.12.

3.6.13 WRITE RAM COMMAND (15H) – 3M DRIVE ONLY PARAMETER BYTES: 5

This is a special diagnostic command used by the 3M Company HCD-75 tape drive. Refer to the 3M HCD-75 user manual for implementation information. Figure 3-11 shows the parameter byte format for the WRITE MEMORY command.

3.6.14 READ RAM COMMAND (16H) – 3M DRIVE ONLY PARAMETER BYTES: 5

This is a special diagnostic command used by the 3M Company HCD-75 tape drive. Refer to the 3M HCD-75 user manual for implementation information. Figure 3-11 shows the parameter byte format for the READ RAM command.

3.6.15 VERIFY COMMAND (17H) – 3M DRIVE ONLY PARAMETER BYTES: 5

The Verify command for the HCD-75 tape drive checks for any data errors via the error detection circuitry. The verification is performed from a beginning track and block number to an ending track and block number. Refer to Figure 3-12 for the format of the VERIFY command parameter bytes.

3.6.16 RUN SELFTEST 1 (18H) – QIC-02 DRIVE ONLY PARAMETER BYTES: 1

This command instructs the tape drive to execute a selftest of its internal hardware. As defined in the QIC-Ø2 specification, this self test does not allow the drive to write to the tape. The status returned from the drive after execution of this command is returned in sense byte 4. Consult the drive manufacturer's manual to decode this byte.

3.6.17 READ EXTENDED STATUS (1AH) – QIC-02 ONLY PARAMETER BYTES: 1

This command informs the drive to return 64 bytes of status information, which is returned verbatim to the host board as sense bytes 4 through 67. These 64 bytes of status information are vendor defined.

3.6.18 SET ALTERNATE SELECT MODE (1BH) - QIC-02 ONLY PARAMTER BYTES: 1

This command instructs the iSBX 217C board to issue the SELECT LOCK CARTRIDGE COMMAND defined in the QIC-Ø2 specification, instead of the normal SELECT COMMAND, whenever the iSBX 217C board needs to select the tape drive. This command must be issued after the RESET command and before the INITIALIZATION command.

3.6.19 RETURN RAW DRIVE STATUS (1CH) - QIC-02 ONLY PARAMETER BYTES: 1

This command returns the six bytes of drive status (as defined by the QIC-Ø2 specification) from the iSBX 217C board to the baseboard. These bytes initially came from the drive to the iSBX 217C board following the last executed command.

3.6.20 RESET BAD PARITY FLAG (20H) - QIC-02 ONLY PARAMETER BYTES: Ø

This command instructs the UPI to reset the Bad Parity Flag in its status register. This command does not require parameter bytes and returns only one sense byte.

3.6.21 START OF TRANSFER (SOT) COMMAND (40H) PARAMETER BYTES: 1

This command must be issued by the host before the start of the data transfer. This action synchronizes the data transfer handshake from the host to the iSBX 217C board. The unit number used in the SOT command must match the unit number in parameter byte Ø, and the EOT command.

3.6.22 END OF TRANSFER (EOT) COMMAND (80H) PARAMETER BYTES: 1

This command must be issued after completing the data transfer. The purpose of the END OF TRANSFER command is to inform the iSBX 217C board that the data transfer is complete. Since the iSBX 217C board does not count the number of bytes transferred during a read or write operation, it would not otherwise know the transfer had finished. The unit number used in the EOT command must match the unit number in parameter byte Ø, and the SOT command.

NOTE

Do not issue the END OF TRANSFER command if the transfer was aborted by the iSBX 217C board (MINTRØ or OBF detected prior to issuing SOT).

3.6.23 PAUSE COMMAND (81H) – QIC–02 ONLY

PARAMETER BYTES: 1

This command can be issued anytime during a READ or WRITE operation, but must occur before an EOT command has been issued. The PAUSE command places the iSBX 217C board in an idle condition, thereby ensuring no signal line will change (ie, INTERRUPT/TDMA). This command is used if the host board cannot accommodate an interrupt or TDMA (Terminate DMA) during a time critical period (ex: when host board is servicing a higher priority interrupt from another device).

CAUTION

Before issuing the PAUSE command to the iSBX 217C board, the Bad Parity Flag in the UPI Status Register must be checked. If the flag indicates bad parity, the RESET BAD PARITY FLAG command must be issued to the iSBX 217C board. Failure to issue the RESET BAD PARITY FLAG command (at this point) will cause a drive fault to be indicated in the sense bytes returned to the host board.

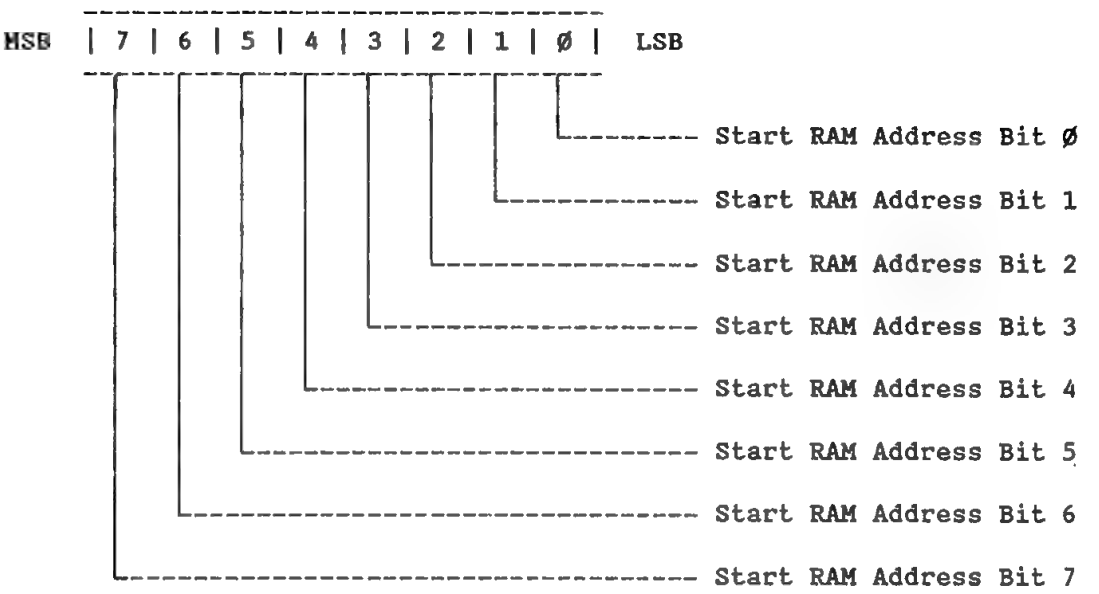
3.6.24 RELEASE PAUSE COMMAND (82H) – QIC–02 ONLY

PARAMETER BYTES: 1

This command must be issued by the host board after a PAUSE command to remove the iSBX 217C board from the idle condition. Once the RELEASE PAUSE command is issued, the iSBX 217C board returns to it's previous operation before the PAUSE command was issued.

READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 1:



READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 2:

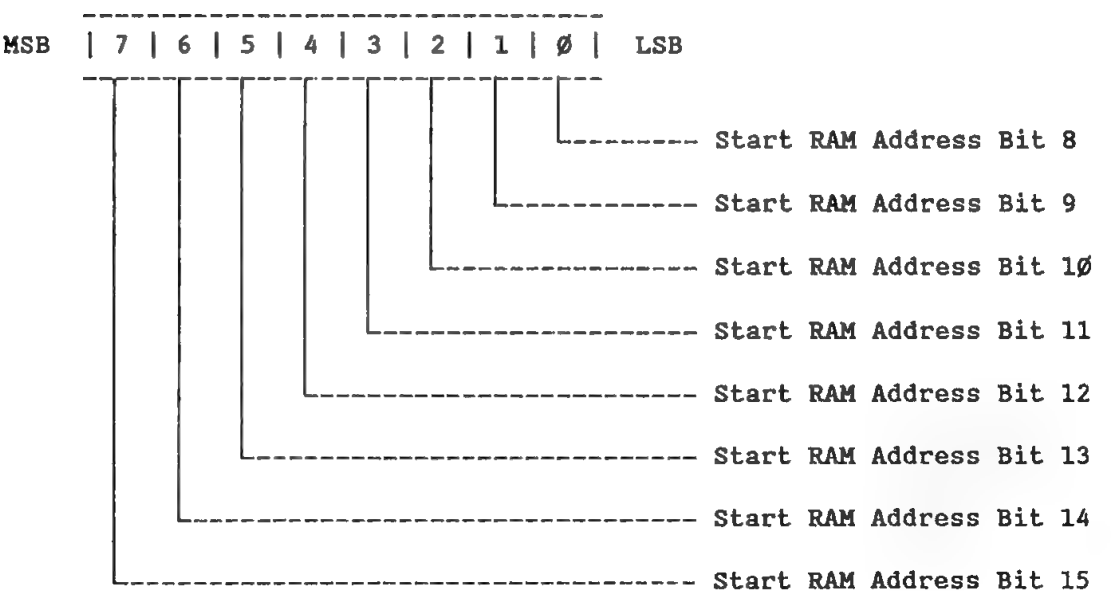
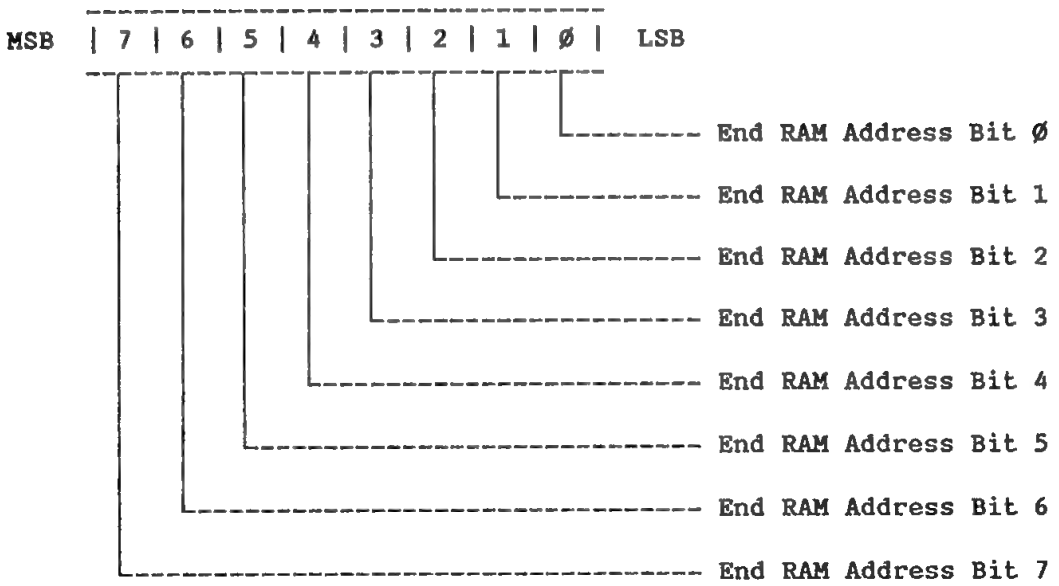


Figure 3-11. READ/WRITE RAM Parameter Bytes
(3M Drive Only)

READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 3:



READ RAM, WRITE RAM COMMANDS

PARAMETER BYTE 4:

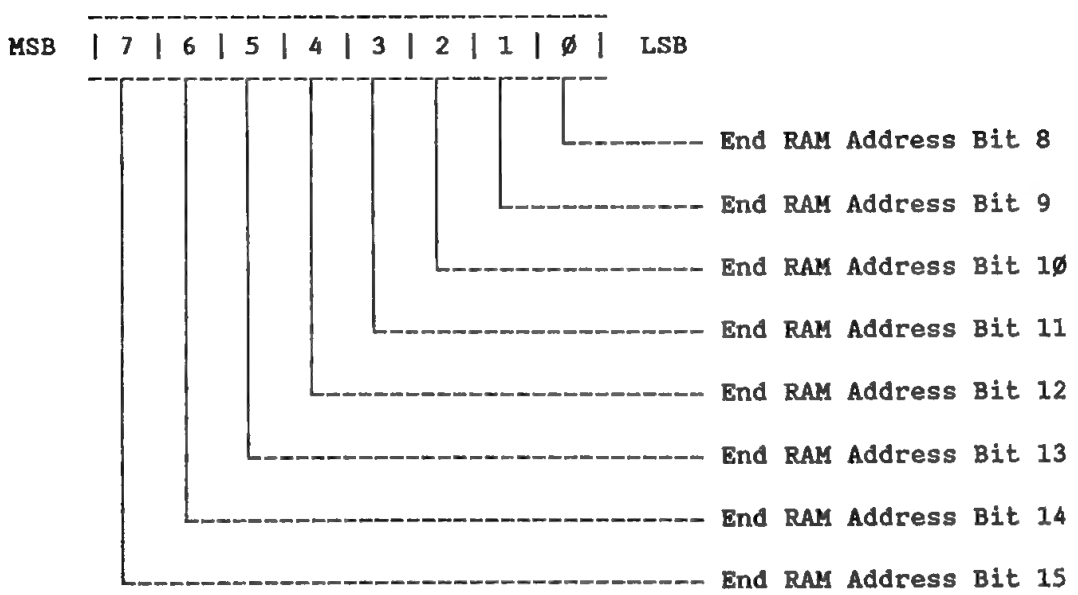
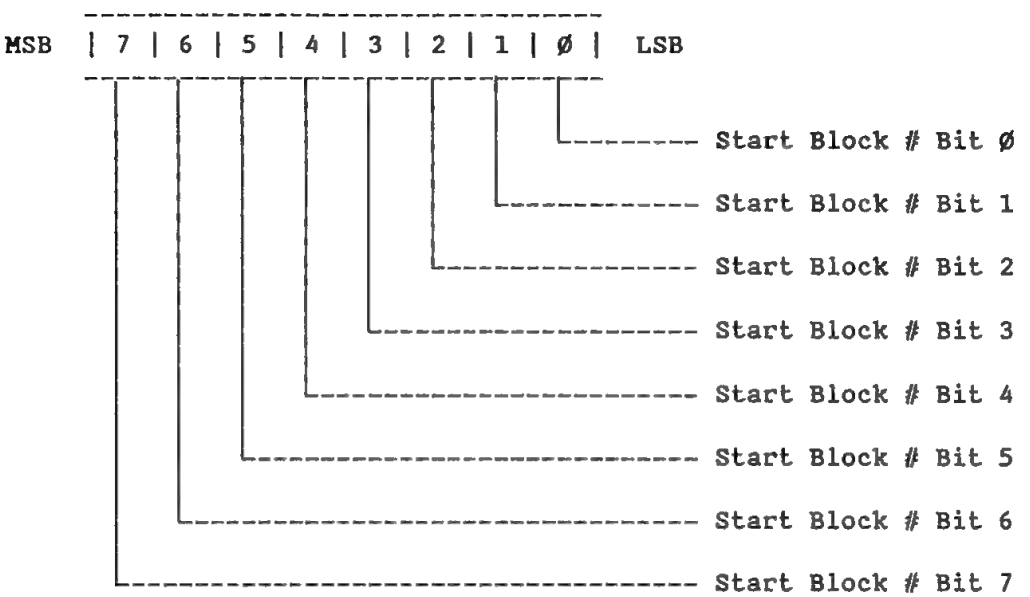


Figure 3-11. READ/WRITE RAM Parameter Bytes (continued)
(3M Drive Only)

VERIFY COMMAND

PARAMETER BYTE 1:



VERIFY COMMAND

PARAMETER BYTE 2:

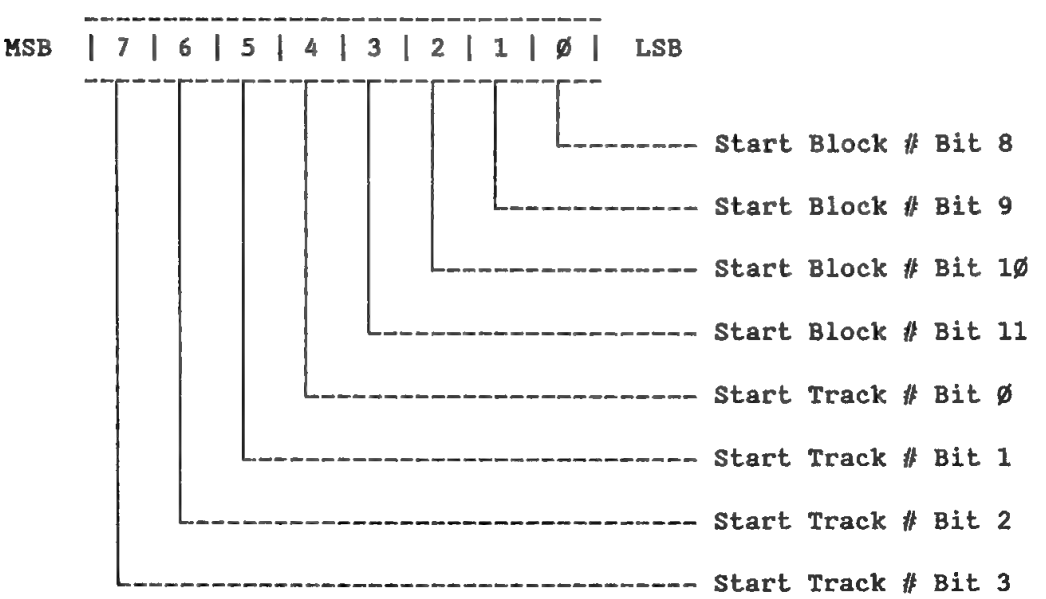
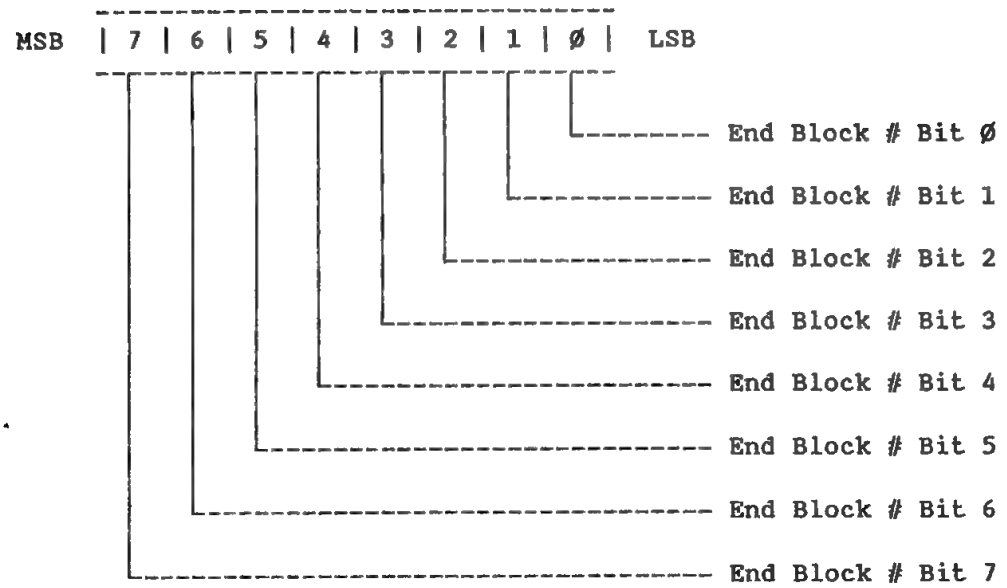


Figure 3-12. VERIFY Command Parameter Bytes (3M Drive Only)

VERIFY COMMAND

PARAMETER BYTE 3:



VERIFY COMMAND

PARAMETER BYTE 4:

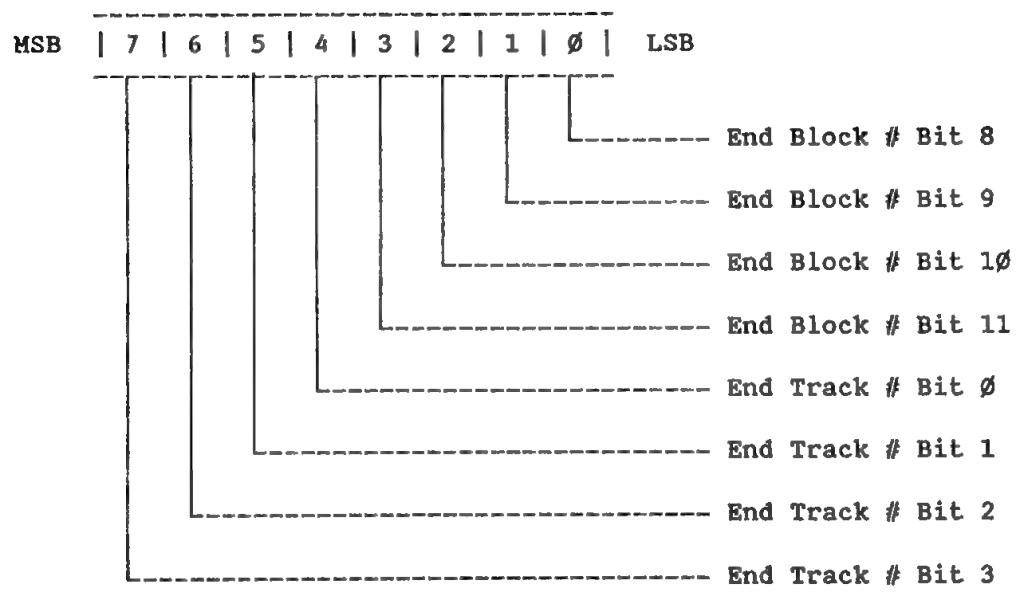


Figure 3-12. VERIFY Command Parameter Bytes (continued)
(3M Drive Only)

3.7 DRIVE SENSE STATUS BYTES

The sense status bytes must be read at the completion of every command. The following paragraphs discuss the status sense bytes. Figures 3-13 through 3-15 define bit functions for these bytes. These bytes are used for error checking and to monitor the results of read or write operations.

The bit definitions for the Sense Status Bytes are shown below:

SENSE BYTE 1:

BØ: Checksum Error is set only for the reset command and means the internal EPROM of the UPI device on the iSBX 217C board is not functioning properly. The host should not use the iSBX 217C board when this bit is set.

B1: The drive not ready bit is set by either of the following sources:

- The drive is not ready, or not on-line;
- The drive has not been initialized.

B2: Hard Data Error is set during a read or write operation when an unrecoverable data error exists.

B3: Soft Data Error is set for each read after write error during a write command or for each read retry for a read command.

B4: Buffer Under-Run Error is set when the host cannot transfer the data fast enough for the QIC-Ø2 drive to operate continuously.

B5: The fault bit is set by any of the following faults:

- Drive is not ready (refer to drive manual);
- Communication failure of any type between iSBX 217C board and the host board;
- Communication failure between iSBX 217C board and the host board when the iSBX 217C board is expecting a SOT command or EOT command, but receives another command.;

B6: Write-Protect bit is set if the drive is write-protected.

B7: Cartridge Not Present bit is set when the drive is empty.

SENSE BYTE Ø:

MSB	7	6	5	4	3	2	1	Ø	LSB

Binary count of the number of sense bytes to be read by the host after Sense Byte Ø:

- For the QIC-Ø2 drive it will always be 3, with the exception of the READ EXTENDED STATUS command which returns 64 bytes of status information (see Section 3.6.17).
- For the 3M drive, it will always be 3 until the INITIALIZATION command is issued; after that, it will always be 5, unless the RESET command is issued.

SENSE BYTE 1:

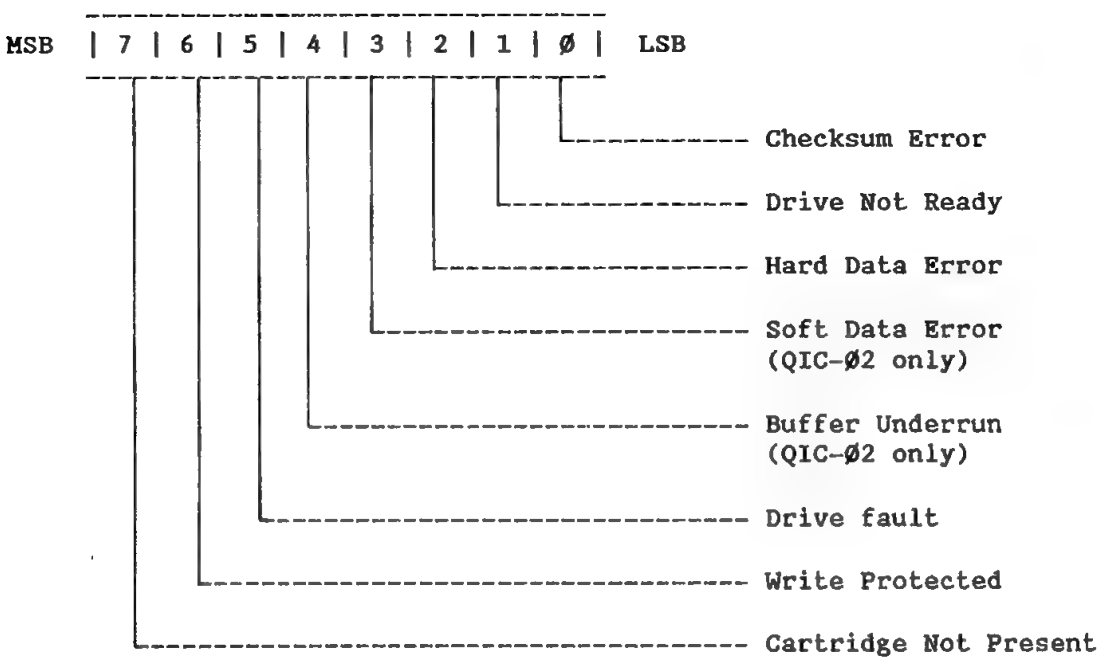
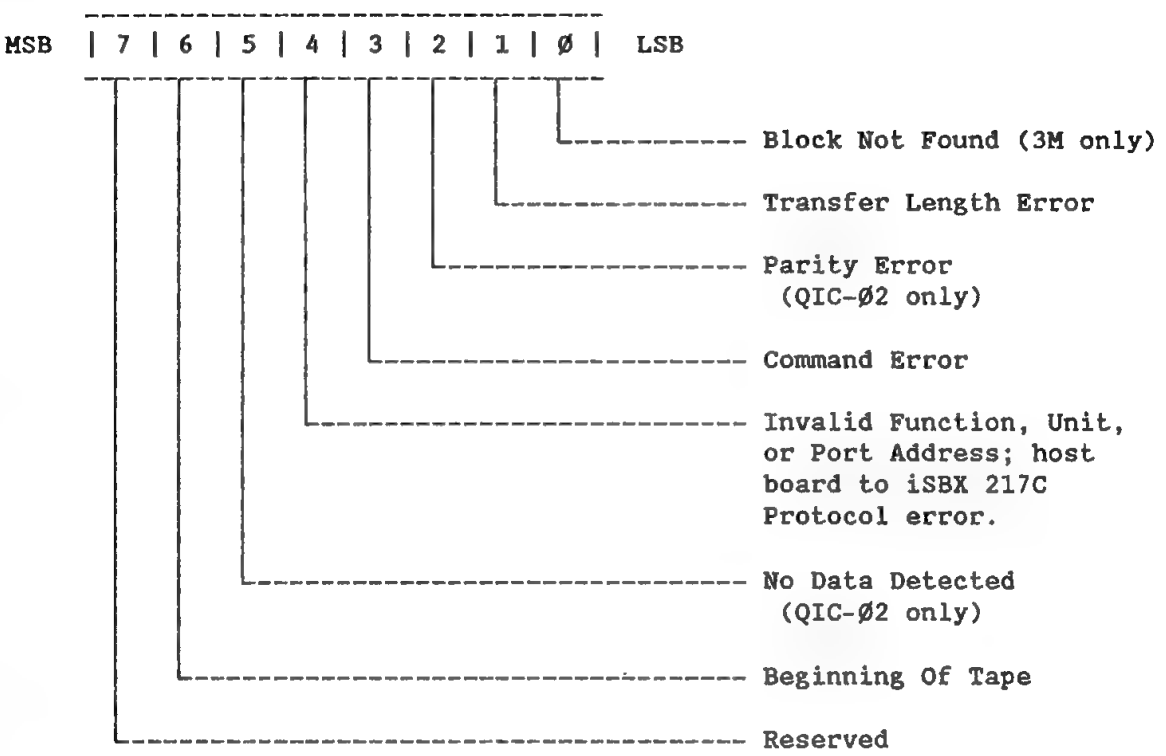


Figure 3-13. Status Sense Bytes Ø and 1

SENSE BYTE 2:



SENSE BYTE 3:

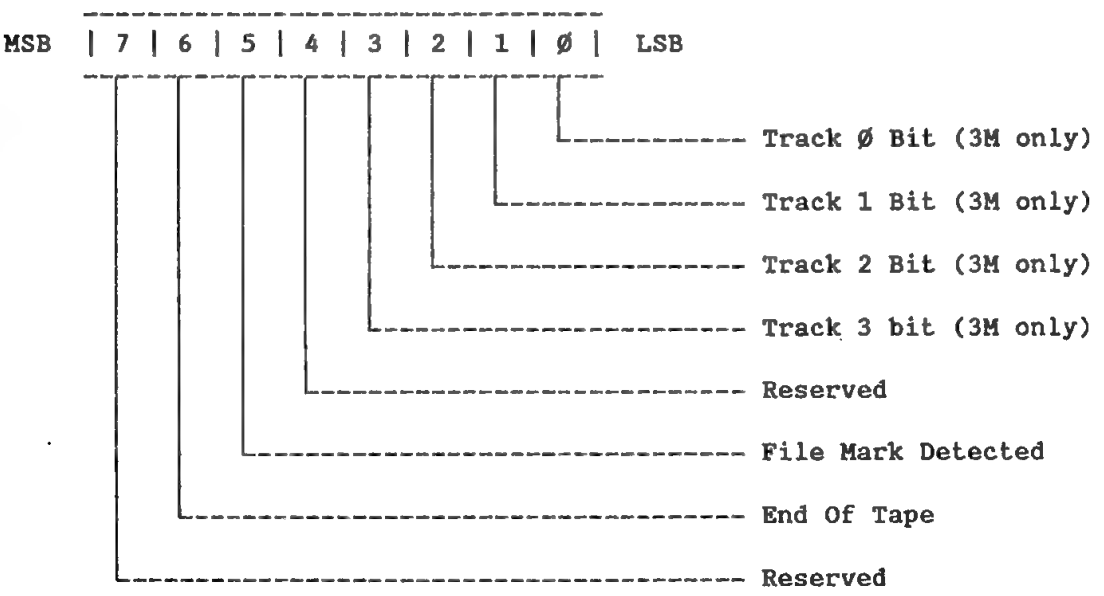
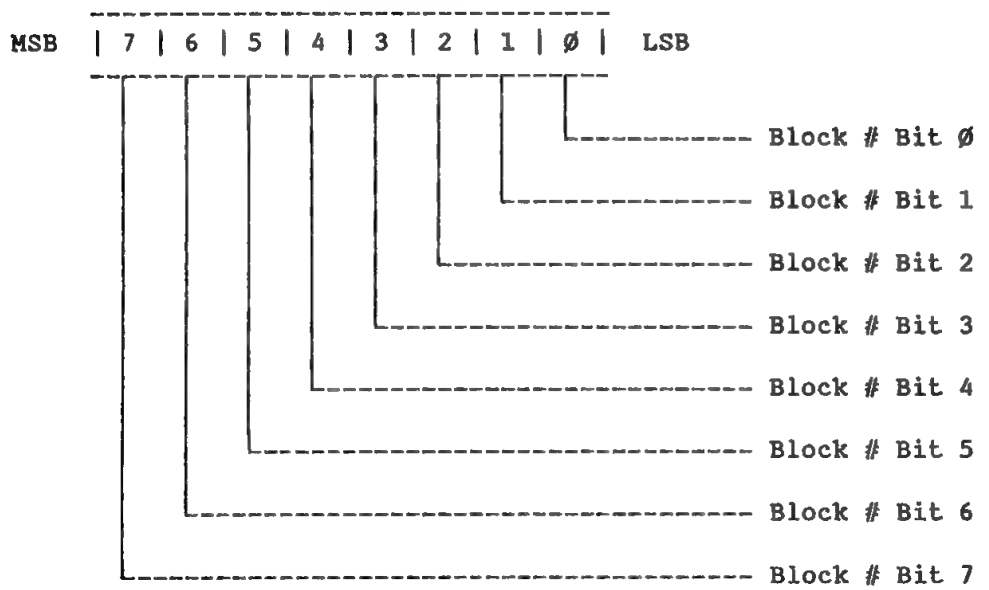


Figure 3-14. Status Sense Bytes 2 and 3

SENSE BYTE 4 (3M DRIVE ONLY):



SENSE BYTE 5 (3M DRIVE ONLY):

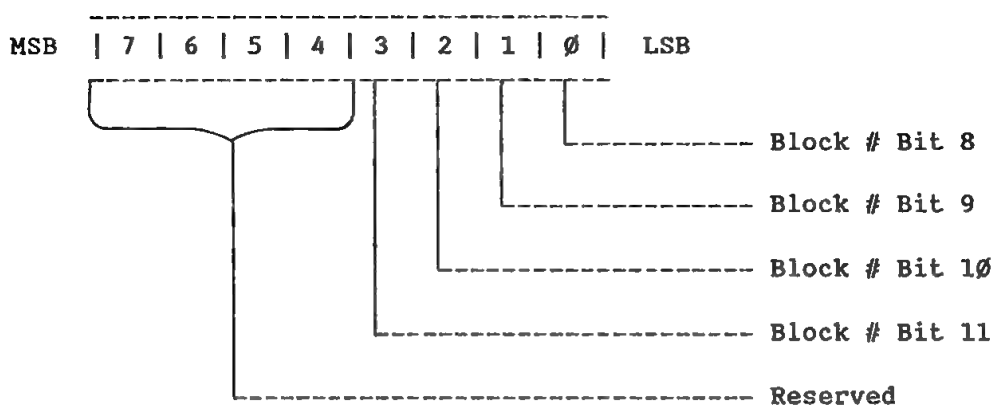


Figure 3-15. Status Sense Bytes 4 and 5

SENSE BYTE 2:

BØ: Block Not Found Error is set when the desired block and track number header key cannot be found; or if the block you are reading is not followed by a file mark or data.

B1: The length error bit is set whenever the drive terminates the data transfer rather than the host board terminating the transfer.

B2: Parity error occurred during data transfer.

B3: Command Error occurs if the drive has detected an invalid command, such as not rewinding one unit before communicating with a second unit (if multiple drives are attached).

B4: Invalid Function, Unit, or Port Address Error means the host has violated the communications protocol with the iSBX 217C board; or when an invalid command (such as issuing a 3M-only command to the QIC-Ø2 drive) is executed.

B5: The No-Data-Detected Error occurs when the drive fails to detect a data block or file mark and times out.

B6: Beginning Of Tape bit. For the QIC-Ø2 drive this bit is set when the tape is rewound and positioned at the logical beginning of tape. For the 3M drive this bit is set when the tape is rewound and positioned at the physical beginning of tape.

B7: Reserved.

SENSE BYTE 3:

BØ: Track Ø Bit.

B1: Track 1 Bit.

B2: Track 2 Bit.

B3: Track 3 Bit.

B4: Reserved.

B5: The file mark bit is set when a file mark has been detected by the drive.

B6: End Of Tape bit. When set, this bit signifies the drive (QIC-Ø2 and 3M) has reached the logical (not physical) end of tape.

B7: Reserved.

SENSE BYTE 4:

BØ - B7: These bits are the least significant 8 bits (bits Ø - 7) of the current block after the operation is completed. During a read operation the block number is valid only if a file mark is detected.

SENSE BYTE 5:

BØ - B3: These bits are bits 8 through 11 of the current block.
B5 - B7: Reserved.

***

CHAPTER 4
SERVICE INFORMATION

4.1 INTRODUCTION

This chapter provides the following service related information:

a. Service assistance information.
b. Parts location diagram.
c. Schematic diagrams.

4.2 SERVICE ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Center in Phoenix, Arizona. Customers outside the United States should contact your sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Center, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is usually silk-screened onto the component side of the board.

c. Serial number of the product. This number is usually stamped onto the component side of the board.

d. Shipping and billing addresses.

e. Purchase order number for billing purposes if your Intel product warranty has expired.

f. Extended warranty agreement information, if applicable.

Use the following numbers for contacting the Intel Product Service Marketing Administration group:

Regional Telephone Numbers:

Western Region:	6Ø2-869-4951
Midwestern Region:	6Ø2-869-4392
Eastern Region:	6Ø2-869-4Ø45
International:	6Ø2-869-4862
Telex Number:	668 - 471
TWX Number:	91Ø - 951 - 133Ø

Always contact the Product Service Marketing Administration group before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Product Service Center, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-24Ø, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Product Service Marketing Administration group personnel.

4.3 SERVICE DIAGRAMS

Figure 4-2 provides schematic diagrams of the iSBX 217C MULTIMODULE Board. The schematic diagrams are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides photocopies of the current schematic diagrams with the board, when it is shipped from the factory. Insert these diagrams into this manual and keep for future reference. In most instances, the diagrams shipped with the board will be identical to those printed in the manual.

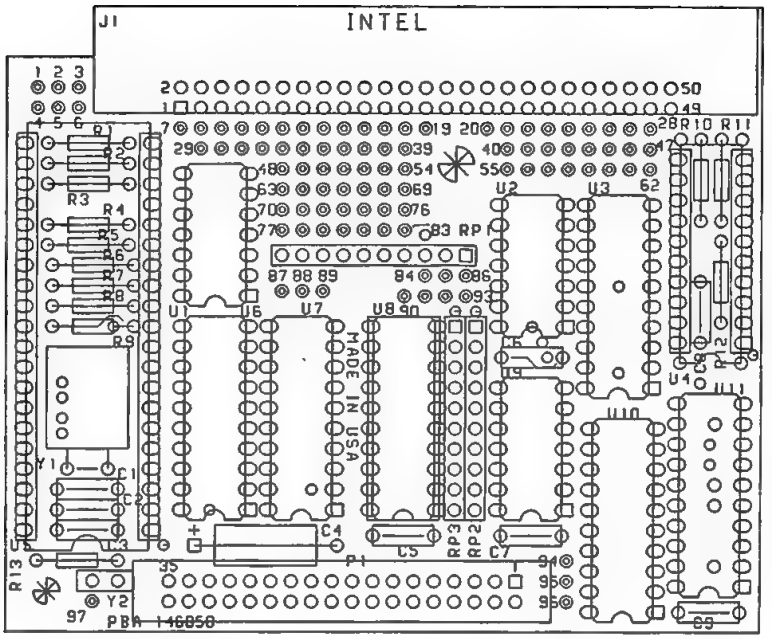
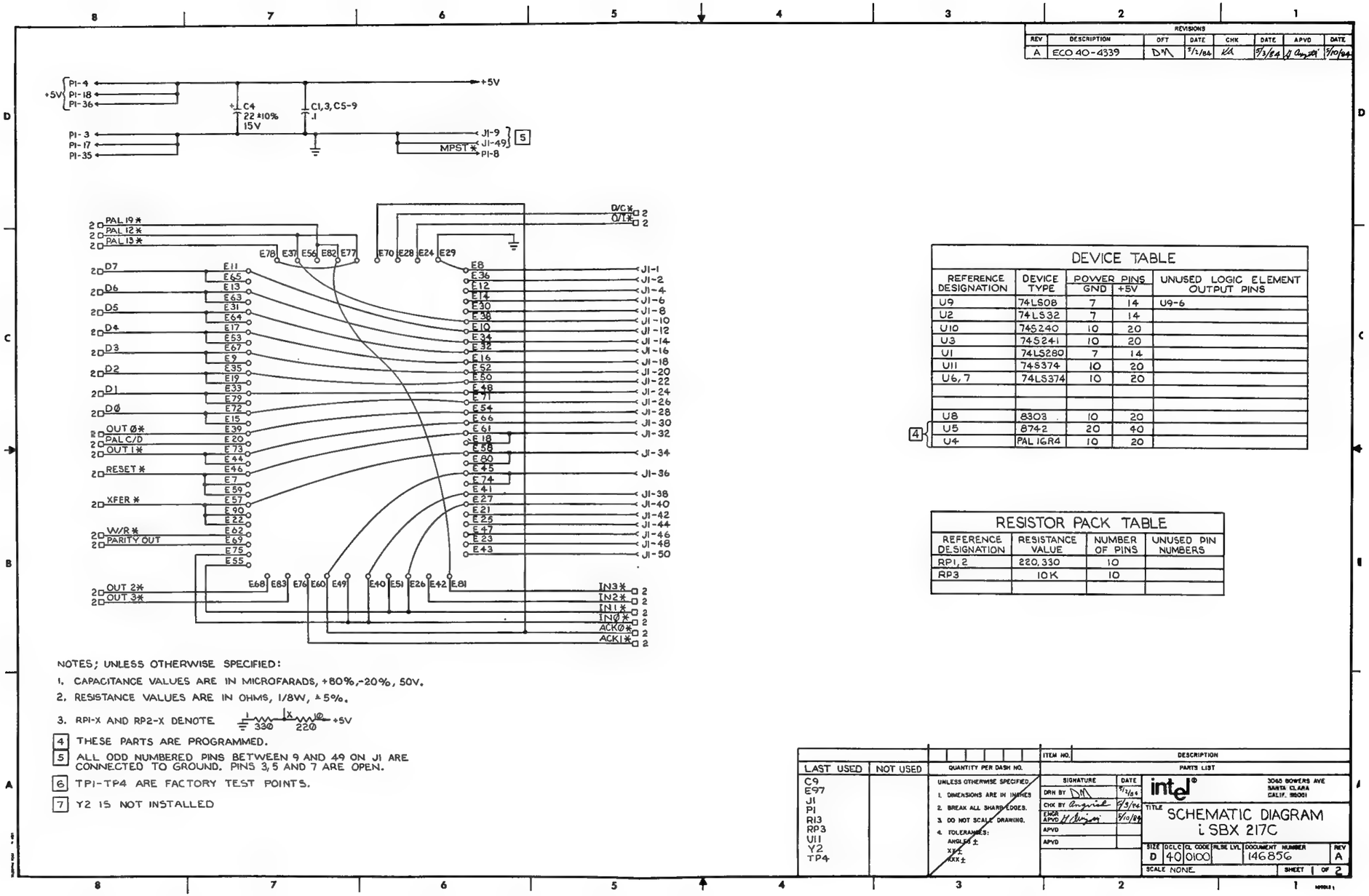


Figure 4-1. Parts Location Diagram



NOTES; UNLESS OTHERWISE SPECIFIED:

1. CAPACITANCE VALUES ARE IN MICROFARADS, +80%,-20%, 50V.
2. RESISTANCE VALUES ARE IN OHMS, 1/8W, ±5%.
3. RP1-X AND RP2-X DENOTE 330 / 220 +5V
4. THESE PARTS ARE PROGRAMMED.
5. ALL ODD NUMBERED PINS BETWEEN 9 AND 49 ON J1 ARE CONNECTED TO GROUND. PINS 3, 5 AND 7 ARE OPEN.
6. TP1-TP4 ARE FACTORY TEST POINTS.
7. Y2 IS NOT INSTALLED

DEVICE TABLE

REFERENCE DESIGNATION	DEVICE TYPE	POWER PINS GND	POWER PINS +5V	UNUSED LOGIC ELEMENT OUTPUT PINS
U9	74LS08	7	14	U9-6
U2	74LS32	7	14	
U10	74S240	10	20	
U3	74S241	10	20	
U1	74LS280	7	14	
U11	74S374	10	20	
U6, 7	74LS374	10	20	
U8	8303	10	20	
4 U5	8742	20	40	
U4	PAL 16R4	10	20	

RESISTOR PACK TABLE

REFERENCE DESIGNATION	RESISTANCE VALUE	NUMBER OF PINS	UNUSED PIN NUMBERS
RP1, 2	220, 330	10	
RP3	10K	10	

LAST USED	NOT USED
C9	
E97	
J1	
P1	
R13	
RP3	
U11	
Y2	
TP4	

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ±, X ±, XX ±, XXX ±

	SIGNATURE	DATE
DRN BY	DM	5/2/84
CHK BY	Engrish	5/9/84
ENGR APVD	H Meijer	5/10/84
APVD		
APVD		

ITEM NO. | DESCRIPTION
PARTS LIST

intel® 3065 BOWERS AVE SANTA CLARA CALIF. 95051

TITLE SCHEMATIC DIAGRAM iSBX 217C

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	0100		146856	A

SCALE NONE SHEET 1 OF 2

Figure 4-2. iSBX™ 217C Schematic Diagram (Sheet 1 of 2)

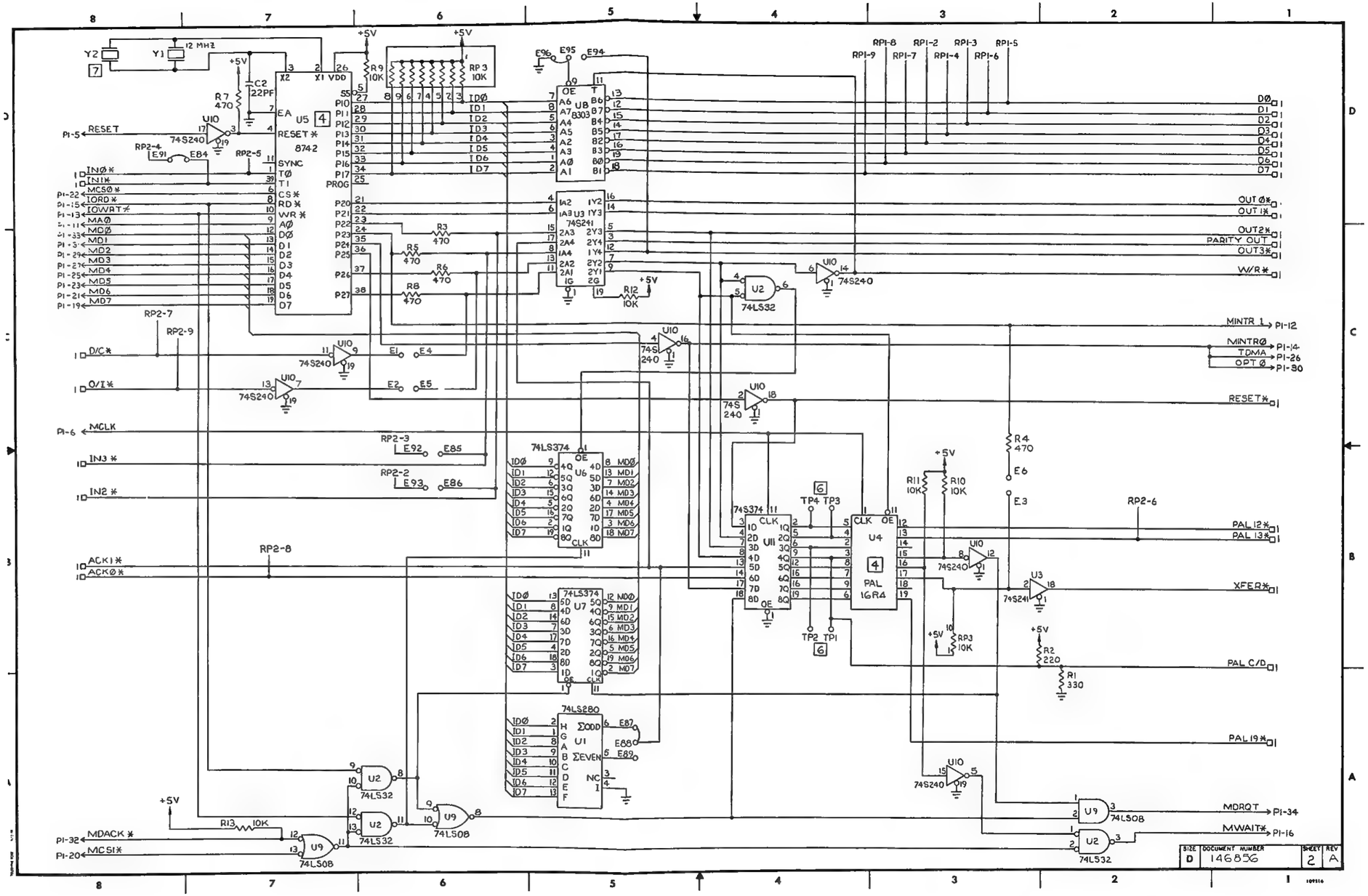


Figure 4-2. iSBX™ 217C Schematic Diagram (Sheet 2 of 2)

***

APPENDIX A
DRIVE ANOMOLIES

During the development of the iSBX 217C board, several minor drive irregularities were discovered. In most cases these drive anomalies will not present any major problems. However, the anomalies are presented here for your reference.

QIC-Ø2 Drive Only:

We discovered only one QIC-Ø2 drive anomaly requiring documentation. When reading a file of unknown length, the host board should wait for 2ØØ milliseconds before issuing the End Of Transfer (EOT) command.

3M Drive Only:

Three anomalies worthy of notation were discovered with the 3M drive.

1. If the drive terminates a read operation due to a file mark, and then the host issues a READ STATUS command for the next command, the drive returns erroneous data. This is true for single and multiple drive configurations.

2. If the host writes 1ØØH to 1FEH (hexadecimal) bytes or 3ØØH to 3FEH bytes in one block, then when reading the same block the byte count will be increased by 2ØØH. That is, (1ØØH to 1FEHH) + 2ØØH; or (3ØØH to 3FEH) + 2ØØH.

3. When writing the last block at the end of the tape (block FFFFH), the drive allows up to an additional 8ØØH (hexadecimal) bytes to be written before the drive terminates the operation. Note that these bytes are lost and cannot be read or recovered.

***

APPENDIX B
3M PAL SOURCE CODE FOR PAL16R6 DEVICE

Table B-1 is the PALASM† source code used in reprogramming a blank PAL16R6 for use when reconfiguring an iSBX 217C board from a QIC-Ø2 interface to a 3M interface.

Table B-1. 3M PAL Source Code for PAL16R6 Device

```
PAL16R6                          PAL DESIGN SPECIFICATION FOR iSBX 217C
PATV101
INTERFACE HANDSHAKE
3M
CLOCK VEND1 TRAN RDWR RESET RDWRSL ACK VEND2 MINTR0 GND /OE /PAL12
/02 /03 /DMAREQ /WSTCNT /XFER /01 /PAL19 VCC

XFER :=   RESET*/RDWR*/TRAN*VEND1*VEND2*ACK*XFER*/WSTCNT*/DMAREQ
        + RESET*/RDWR*/TRAN*VEND1*VEND2*ACK*RDWRSL*/XFER*/DMAREQ*WSTCNT
        + RESET*RDWR*/TRAN*VEND1*VEND2*/ACK*/RDWRSL*/WSTCNT*/03
        + RESET*RDWR*/TRAN*VEND1*VEND2*/ACK*RDWRSL*/WSTCNT*/03
        + RESET*RDWR*/TRAN*VEND1*VEND2*/ACK*RDWRSL*/XFER*/DMAREQ*WSTCNT*03
        + RESET*RDWR*/TRAN*VEND1*VEND2*02*/ACK
        + RESET*/TRAN*/VEND1*/03

DMAREQ :=  RESET*/RDWR*/TRAN*VEND1*VEND2*ACK*RDWRSL*/XFER*/WSTCNT
      + RESET*RDWR*/TRAN*VEND1*VEND2
        */RDWRSL*/ACK*/WSTCNT*/03*/DMAREQ*/XFER
        + RESET*RDWR*/TRAN*VEND1*VEND2*RDWRSL*ACK*DMAREQ*/WSTCNT
        + RESET*RDWR*/TRAN*VEND1*VEND2*RDWRSL*/ACK*/02
        + RESET*/RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/WSTCNT*/03*/02
        + RESET*RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/WSTCNT*/03*01*/02
        + RESET*RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/WSTCNT*/03*/01*02
        + RESET*RDWR*/TRAN*/VEND1
        */RDWRSL*/ACK*/DMAREQ*/WSTCNT*/03*01*/02

WSTCNT :=  RESET*/RDWR*/TRAN*VEND1*VEND2*ACK*/RDWRSL*/XFER
        + RESET*RDWR*/TRAN*VEND1*VEND2*ACK*/RDWRSL*XFER*/WSTCNT*/03
        + RESET*RDWR*/TRAN*VEND1*VEND2*ACK*/RDWRSL*WSTCNT*/XFER*/03
        + RESET*RDWR*/TRAN*VEND1*VEND2*/XFER*/RDWRSL*03
        + MINTR0
        + RESET*/RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*/03
        + RESET*RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*/03*01
        + RESET*RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*/03*02
```

(† = PALASM is a registered trademark of Monolithic Memories, Inc.)

Table B-1. 3M PAL Source Code for PAL16R6 Device (continued)

```
Ø3 :=     RESET*RDWR*/TRAN*VEND1*VEND2*ACK*RDWRSL*DMAREQ*/WSTCNT
        +  RESET*RDWR*/TRAN*VEND1*VEND2*/RDWRSL*/XFER*Ø3
        +  RESET*RDWR*/TRAN*VEND1*VEND2*/ACK*/XFER*DMAREQ*/WSTCNT*Ø3
        +  RESET*/RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/DMAREQ*/WSTCNT*/Ø1*Ø2
        +  RESET*/RDWR*/TRAN*/VEND1*Ø3*/ACK
        +  RESET*RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/DMAREQ*WSTCNT
           */Ø3*Ø1*Ø2
        +  RESET*RDWR*/TRAN*/VEND1*/ACK*Ø3

Ø2 :=     RESET*RDWR*/TRAN*VEND1*VEND2*/DMAREQ*/WSTCNT*XFER*/Ø3
        +  RESET*/RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*Ø1
        +  RESET*/RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/Ø3*Ø2
        +  RESET*RDWR*/TRAN*/VEND1
           *RDWRSL*/ACK*/DMAREQ*WSTCNT*/Ø3*Ø1*/Ø2
        +  RESET*RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/Ø1*Ø2
        +  RESET*RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*Ø2
        +  RESET*TRAN*/VEND2*VEND1*Ø1
        +  RESET*TRAN*/VEND1*Ø2*/VEND2

Ø1 :=     RESET*/RDWR*/TRAN*/VEND1
           *RDWRSL*/ACK*/DMAREQ*WSTCNT*/Ø3*/Ø1*/Ø2
        +  RESET*/RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/WSTCNT*/Ø3*Ø1*/Ø2
        +  RESET*/RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*/Ø3*Ø1
        +  RESET*RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/WSTCNT*/Ø3*/Ø2
        +  RESET*RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*/Ø3
        +  RESET*TRAN*/VEND1*/VEND2*/Ø2
        +  RESET*TRAN*Ø1*/VEND2*VEND1

IF (VCC)  PAL19 = RESET*/RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/DMAREQ
           */WSTCNT*/Ø3*Ø1*/Ø2
        +   RESET*/TRAN*RDWR*/VEND1*/DMAREQ*/WSTCNT
           */Ø2*/Ø3
        +   RESET*/TRAN*RDWR*/VEND1*RDWRSL*/ACK*/WSTCNT
           */Ø3*PAL19
        +   RESET*TRAN*/VEND1*/VEND2*Ø1*/Ø2

IF (VCC)  PAL12 = RESET*/RDWR*/TRAN*/VEND1*RDWRSL*/ACK*/DMAREQ
           */WSTCNT*/Ø3*/Ø1*Ø2
        +   RESET*RDWR*/TRAN*/VEND1*/RDWRSL*/ACK*/Ø3*Ø1*/Ø2
           */DMAREQ*WSTCNT
        +   RESET*RDWR*/TRAN*/VEND1*RDWRSL*/ACK*PAL12
        +   RESET*TRAN*/VEND1*/VEND2*/Ø1*Ø2


DESCRIPTION:

This pal controls the data transfer handshake between the
host baseboard and the tape drive.
;
;
```

***

***

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